T13M SCHEMATIC Revision 1.1

PAGE	Content

SYSTEM PAGE REF.

4	AMD S1 CPU(1)-HT&MISC
5	AMD S1 CPU(2)-DDRII
6	AMD S1 CPU(3)-POWER&GND
7	Fan CTRL/THERMAL SENSOR
8	DDR2 SO-DIMM_0
9	DDR2 SO-DIMM_1
10	DDR2 ADDRESS TERMINATION
11	C51MV HT TO CPU
12	C51MV HT TO MCP
13	C51MV PCIEx16
14	C51MV VGA&LVDS
15	C51MV POWER&GND
16	CRT CONN
17	LVDS & INVERTER CONN
18	MCP51_HT TO C51MV
19	MCP51_PCI I/F
20	MCP51_SATA&IDE&LAN
21	MCP51_USB&GPIO&MISC
22	MCP51_POWER&GND
23	HDD & CD-ROM CONN
24	USB PORTS
25	B/T & F/P
26	B To B CONN(M)
27	EMPTY
28	EMPTY
29	LAN PHY RTL8201CL(10/100)
30	AZALIA - ALC660-GR
31	AUDIO_AMPLIFIER
32	MICROPHONE
33	NEW CARD
34	EC-IT8510E
35	ISA ROM & KB
36	Card Reader GL817E
37	DISCHARGE
38	Instant Key & FFC CONN
39	LEDs
40	EMPTY
41	EMPTY
42	EMPTY
43	EMPTY
44	EMPTY
45	DC & BAT IN
46	SREW HOLE
47	SCH Information
48	History(1)
49	History(2)

PAGE	Content

POWER PAGE REF.

50	POWER_VCORE
51	POWER_SYSTEM
52	POWER_I/O_1.8V & 1.05VS
53	POWER_I/O_DDR & VTT
54	POWER_I/O_VTT & +2.5VS
55	POWER_VGA_CORE(Empty)
56	POWER_VGA_RAM(Empty)
57	POWER_CHARGER
58	POWER_PIC(Empty)
59	POWER_DETECT
60	POWER_PROTECT
61	POWER_LOAD SWITCH
62	POWER_FLOWCHART
63	POWER_SIGNAL

<Variant Name>

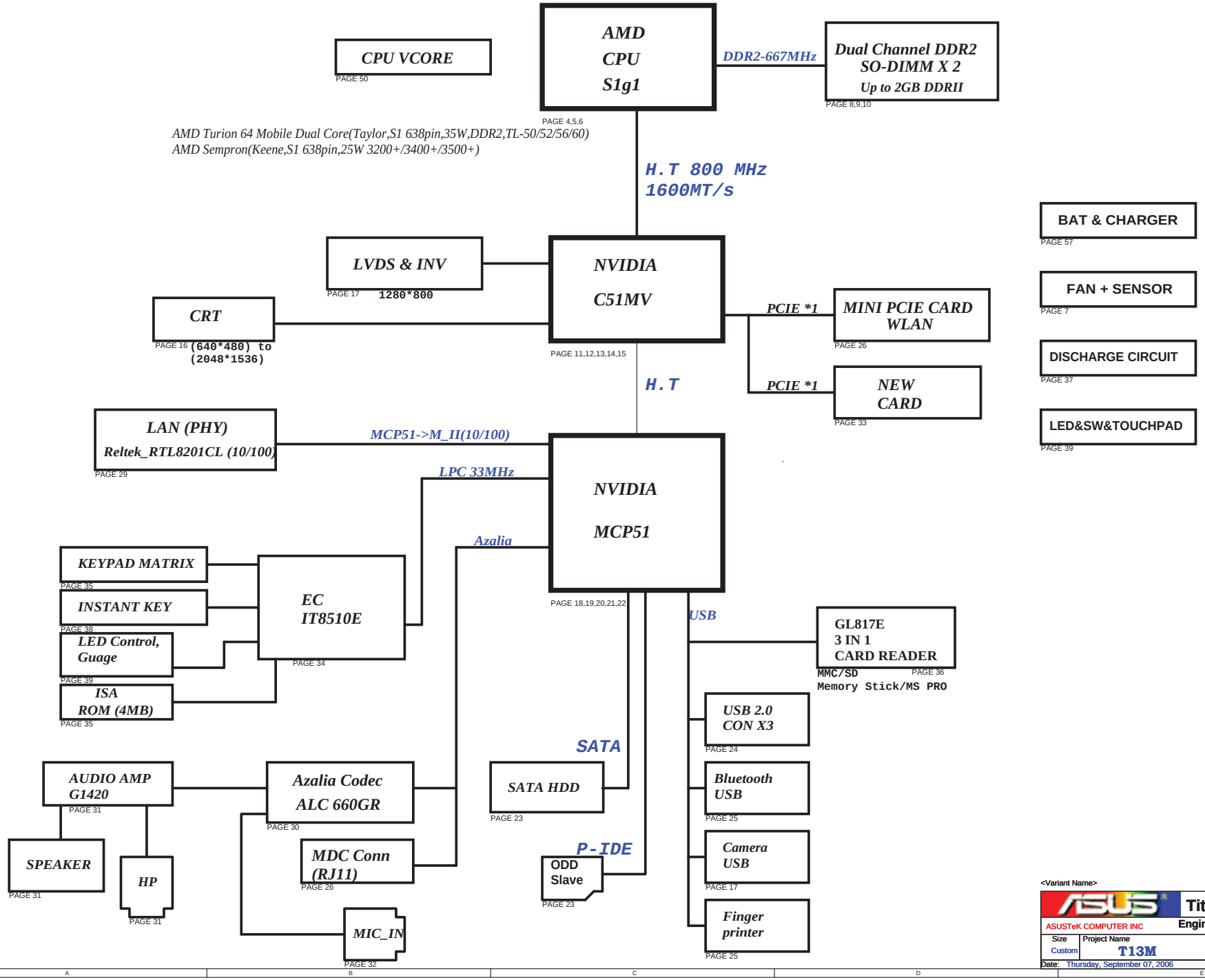
ASUSTeK COMPUTER INC

Title : PAGE REF.

Engineer: CH_LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 1 of 65



<Variant Name>

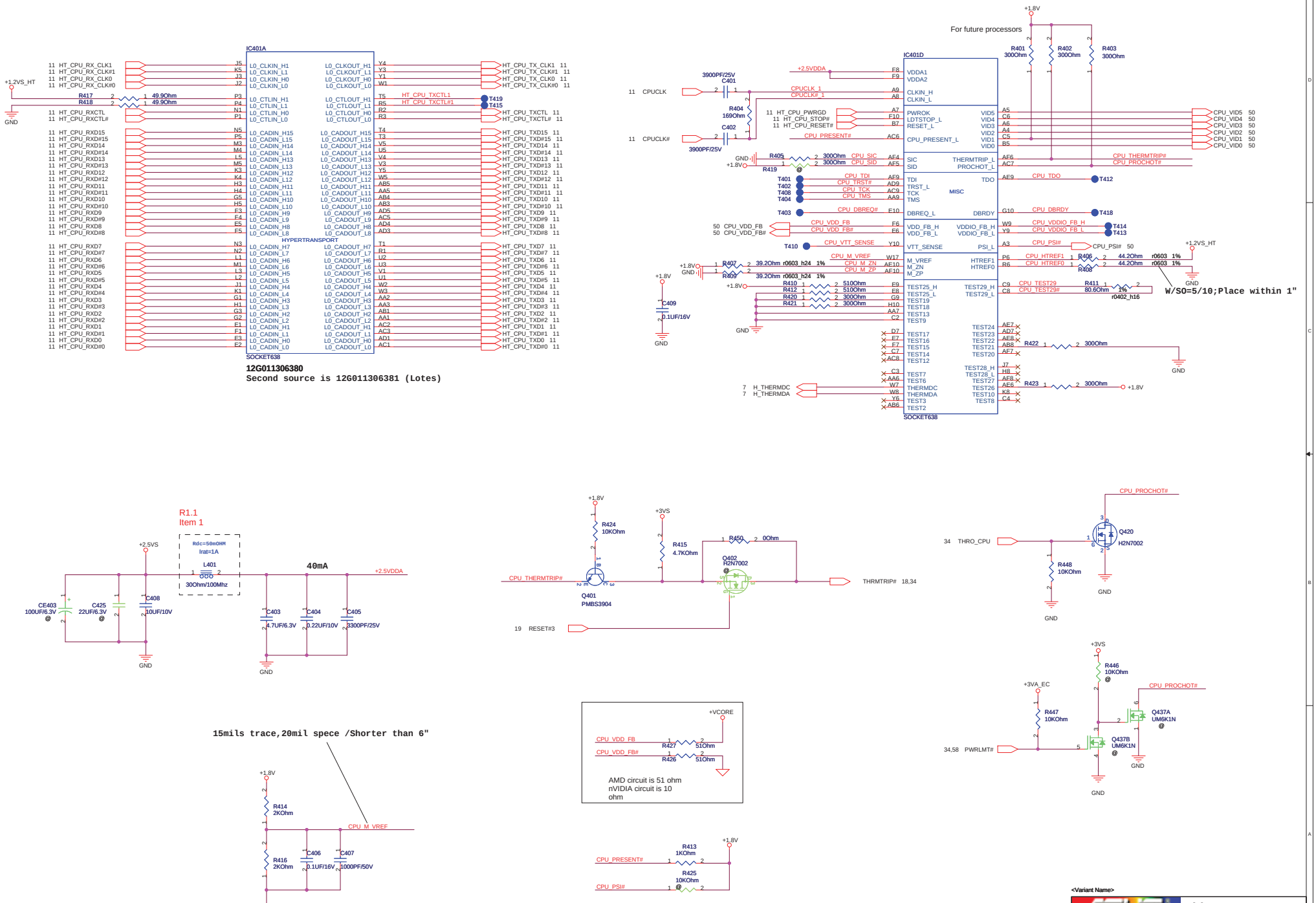
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 3 of 65



<Variant Name>

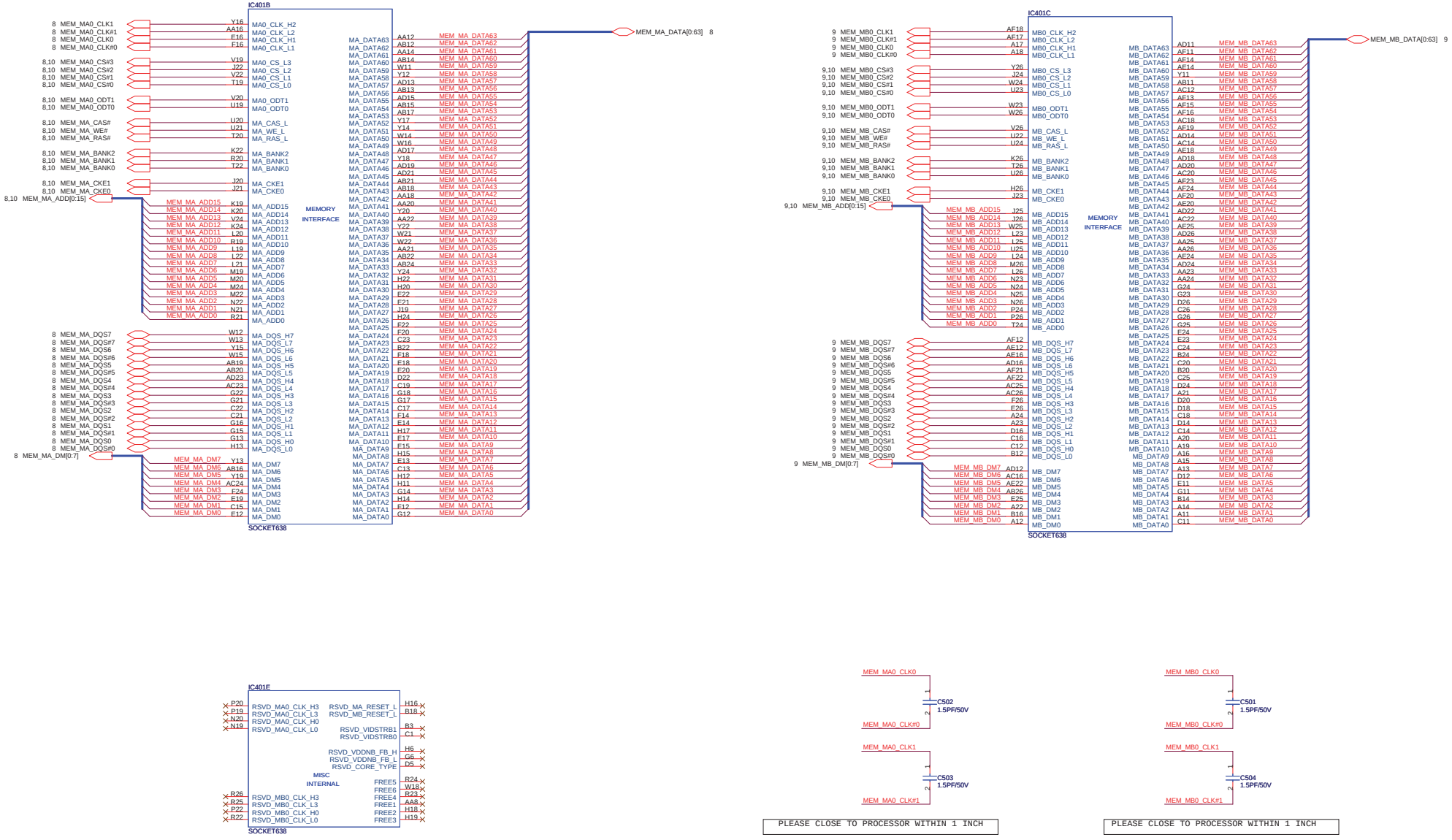
ASUSTeK COMPUTER INC

Title : AMD S1 CPU(1)-HT&MISC

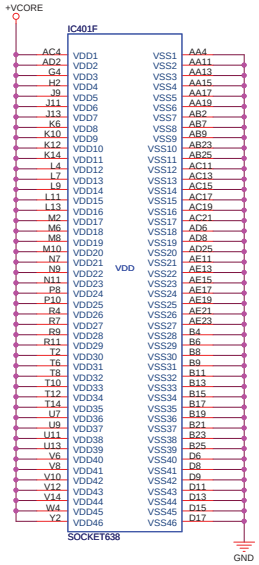
Engineer: CH_LIN

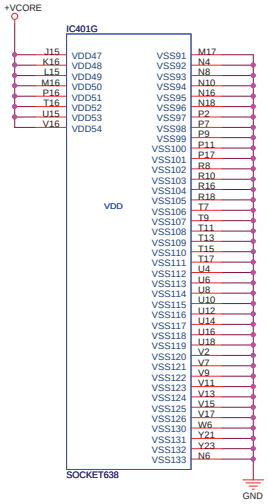
Size	Project Name	Rev
C	T13M	1.1

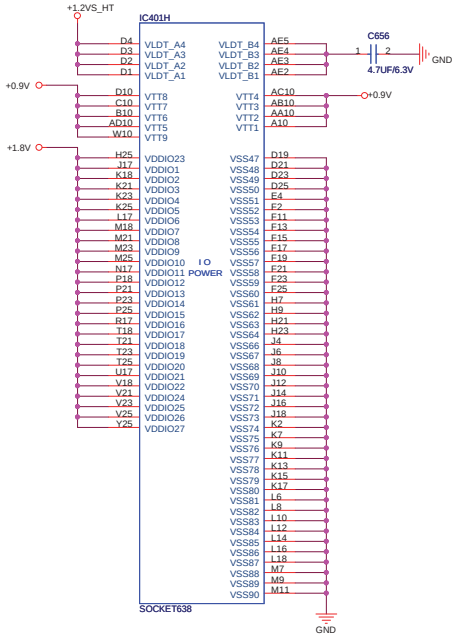
Date: Friday, September 08, 2006 Sheet 4 of 65

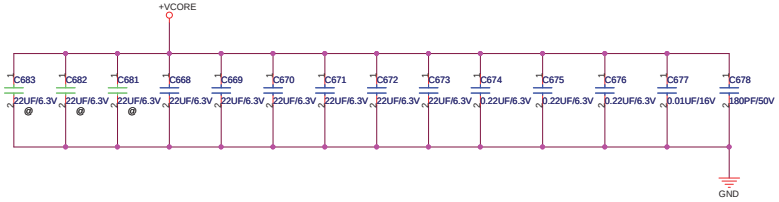


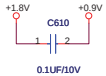
Title :	AMD S1 CPU(2)-DDRII
ASUSTeK COMPUTER INC	Engineer: CH_LIN
Size: C	Project Name: T13M
Rev: 1.1	
Date: Friday, September 08, 2006	Sheet 5 of 65

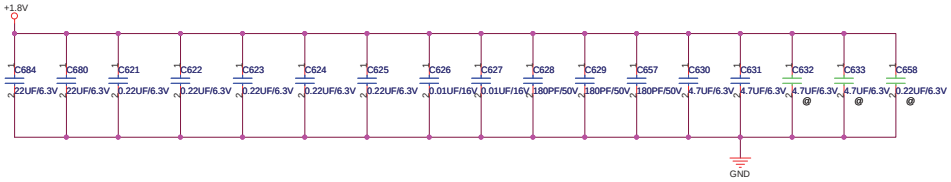


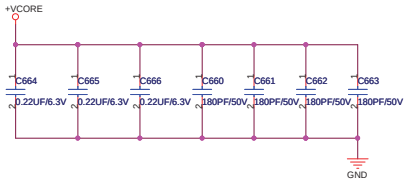


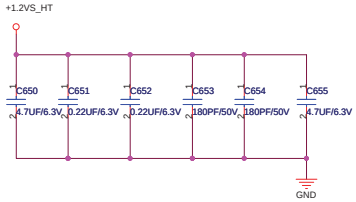


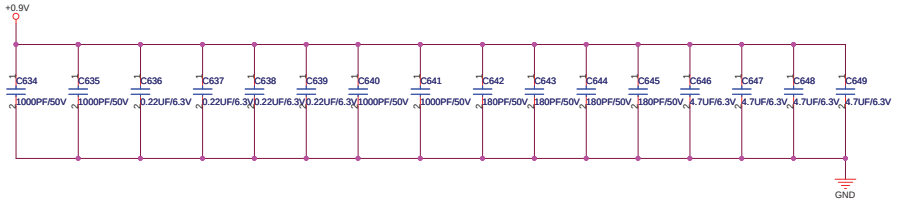






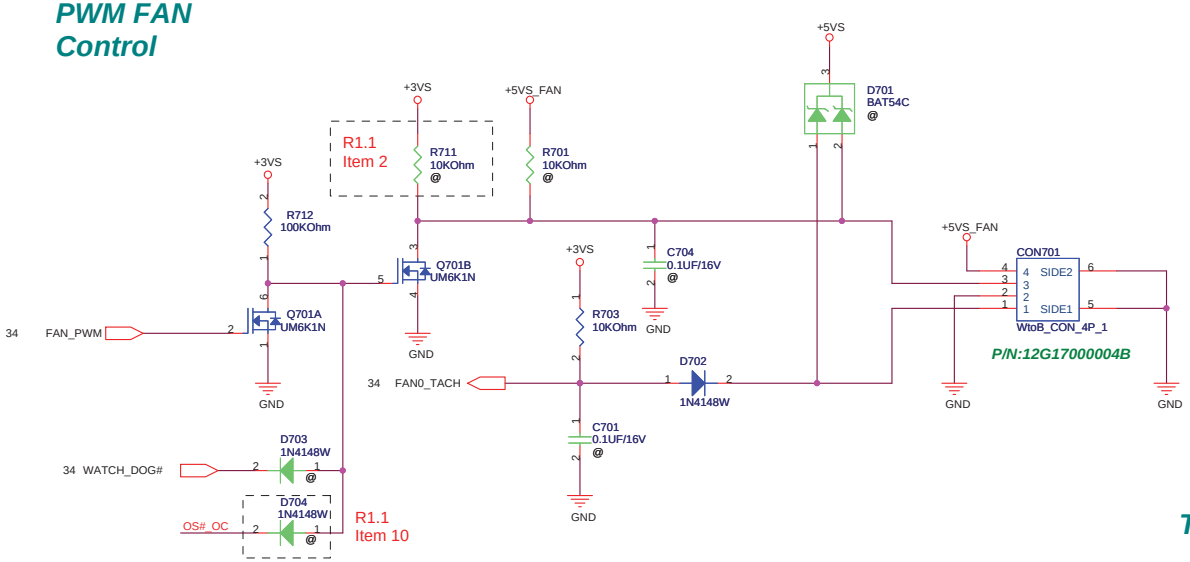


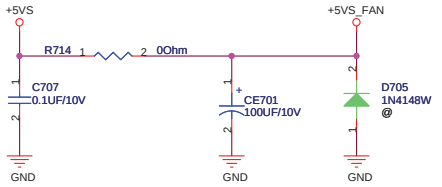




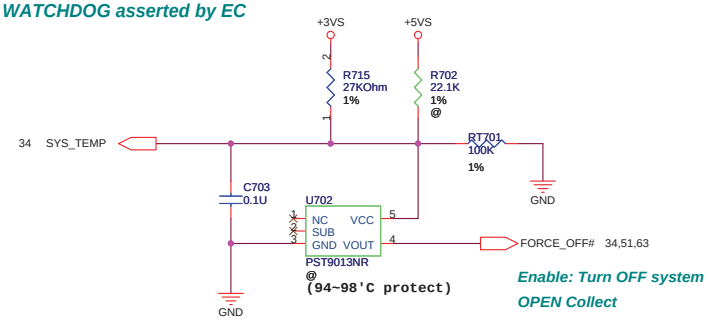
ASUSTeK COMPUTER INC	Title :	AMD S1 CPU(3)-POWER&GND
	Engineer:	CH_LIN
Size: C	Project Name: T13M	Rev: 1.1
Date: Thursday, September 07, 2006	Sheet 6 of 65	

PWM FAN Control

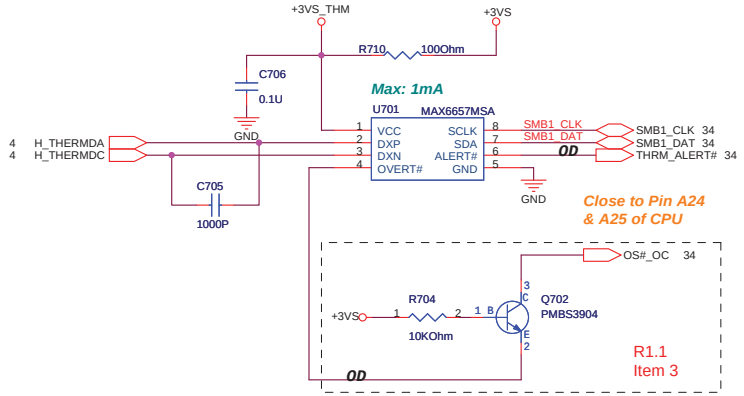




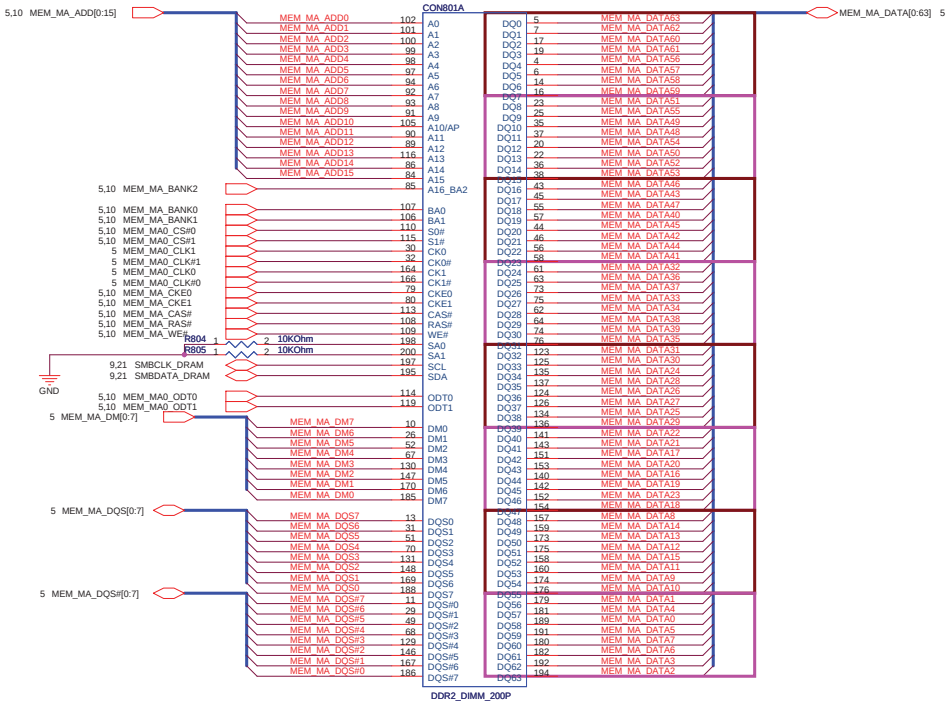
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC



Thermal Sensor

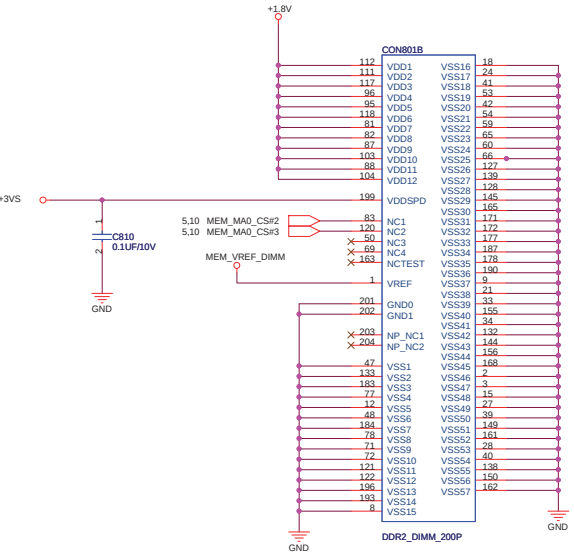


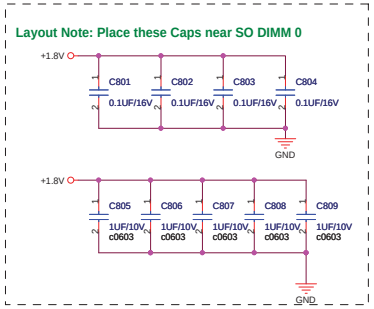
DDR2 DIMM 0

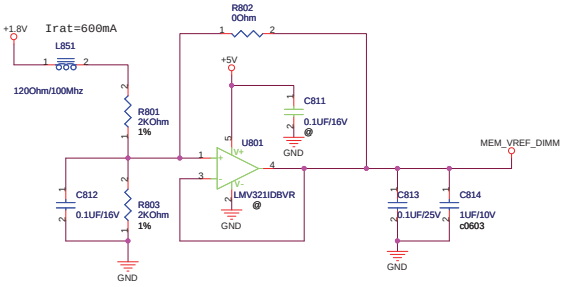


Hight: 4.0 mm

P/N:12G025C22004







Nearby SO-DIMM

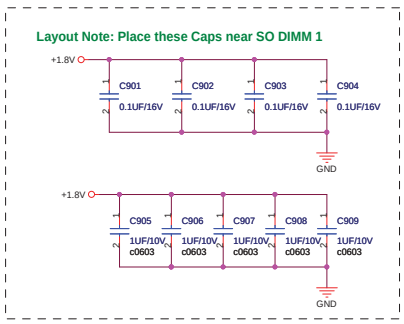
ASUSTeK COMPUTER INC	Title : DDR2_SO_DIMM-0	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 8 of 65	

DDR2 DIMM 1

N.V suggest to change SA0=HI,SA1=LO(Slave address=A2) But F3T BIOS modify OK now.

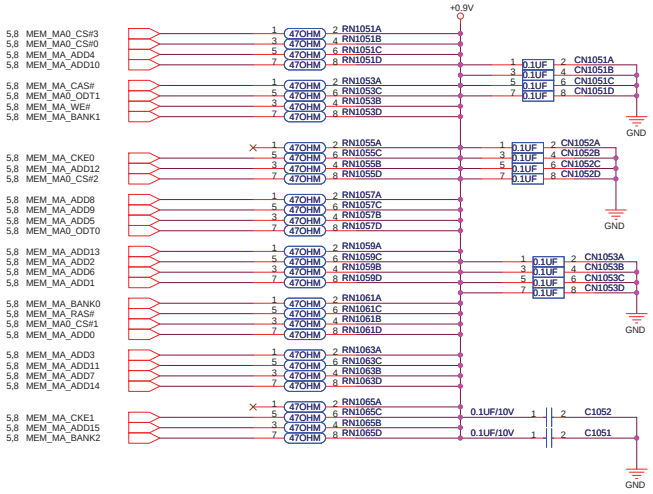
Hight: 9.2 mm

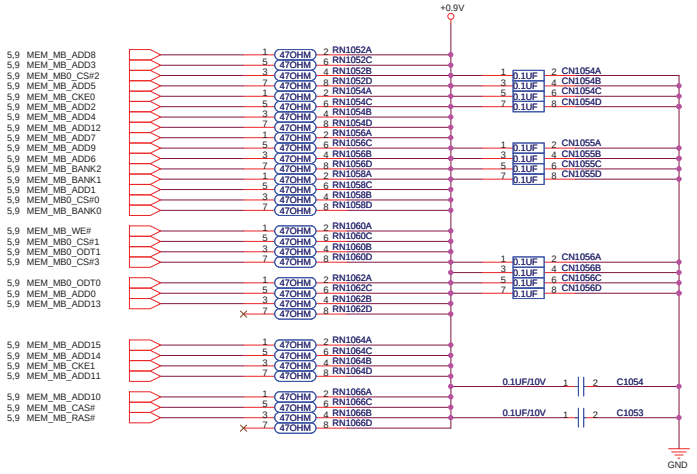
P/N:12G025C22004



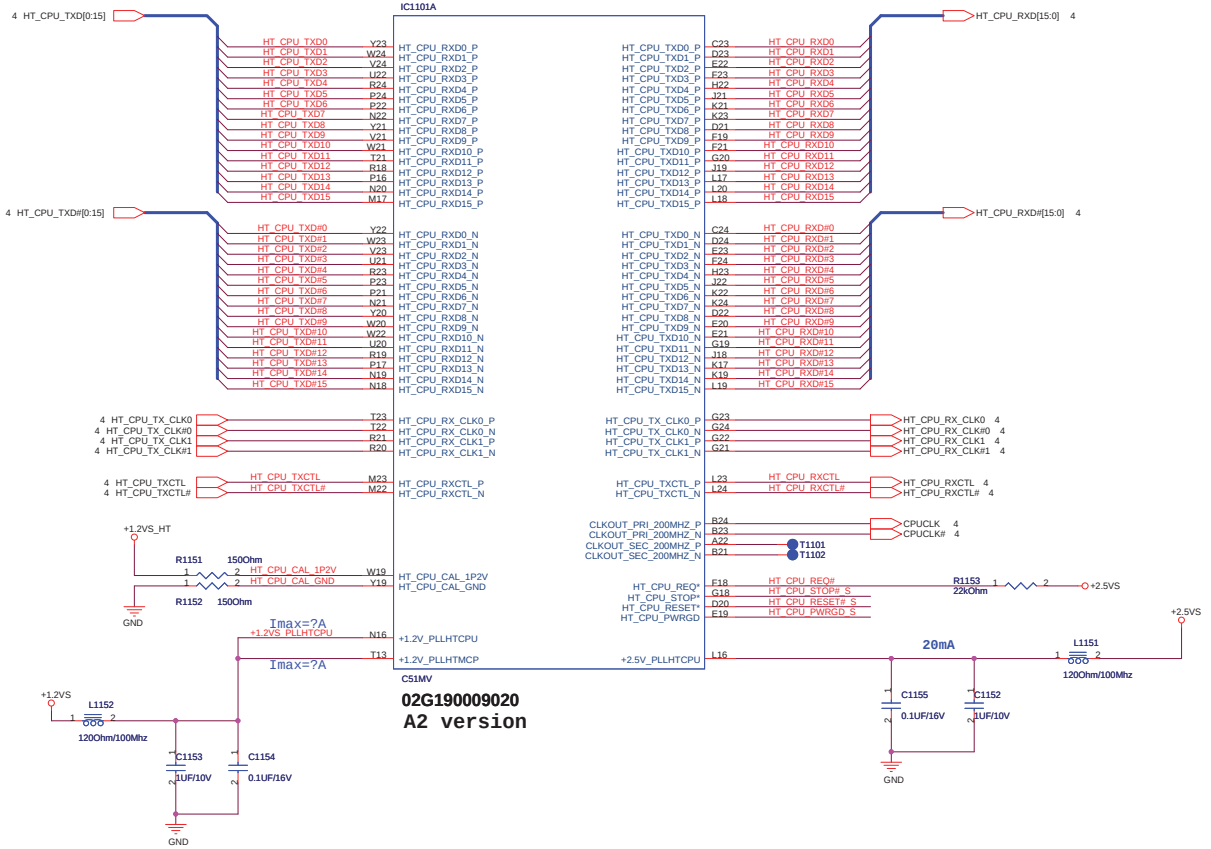
ASUSTeK COMPUTER INC	Title : DDR2_SO_DIMM-1	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 9 of 65	

DIMM TERMINATION

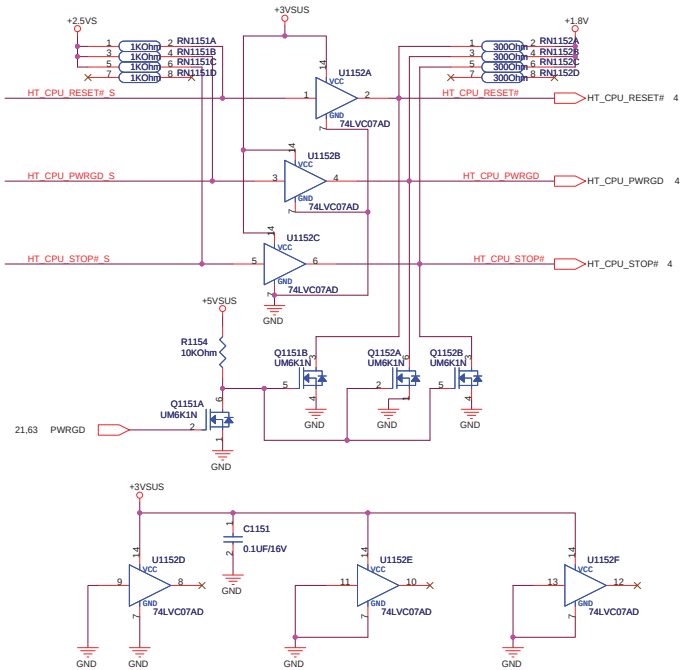


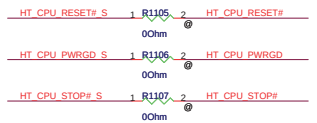


ASUSTeK COMPUTER INC	Title: DDR2_SODIMMS TERMINATIONS	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 10 of 65	

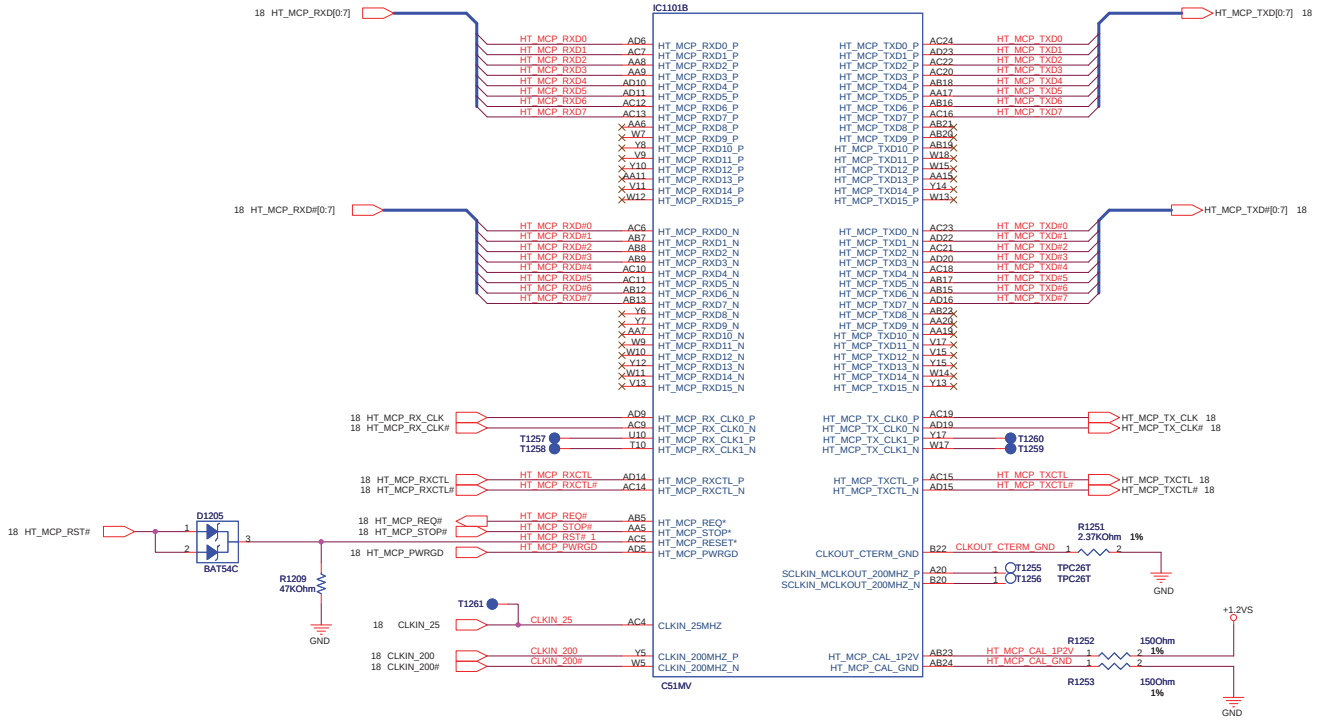


nVidia C51 Chipset side-band signal glitch issue solution.



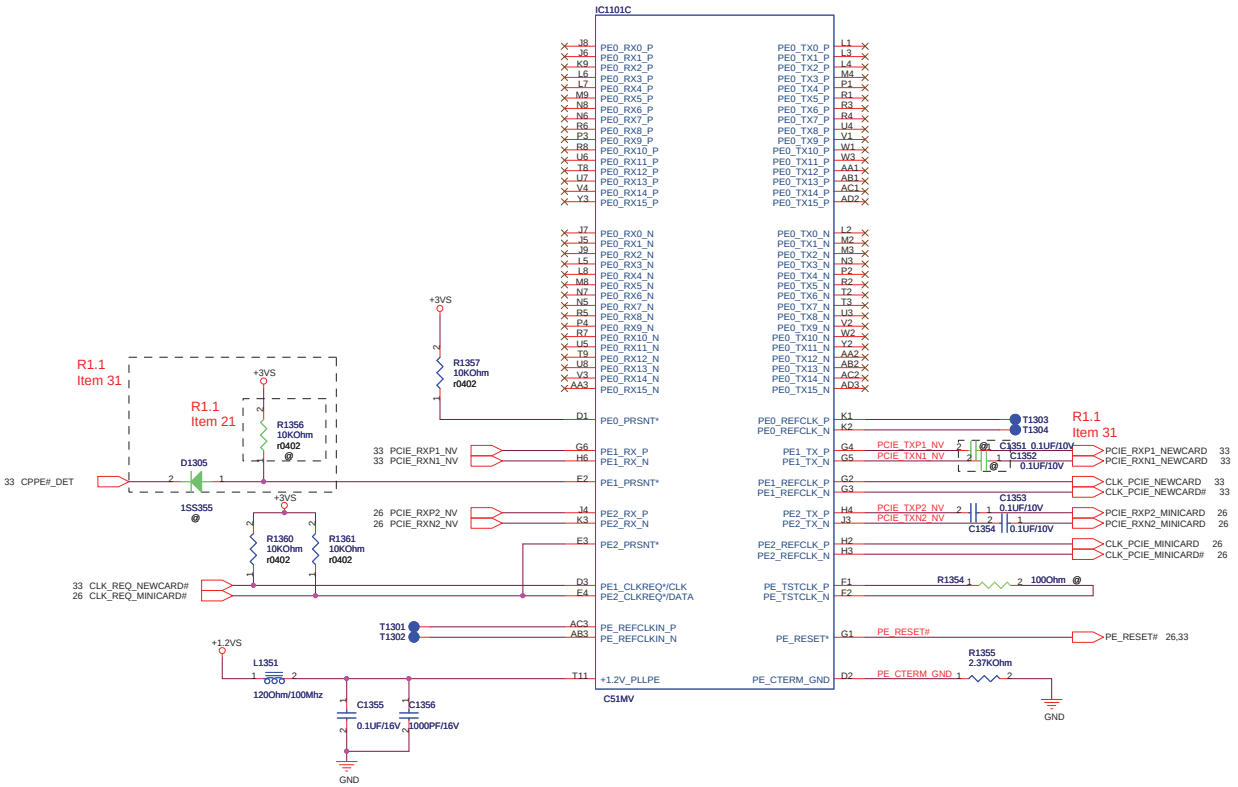


Title : C51MV HT TO CPU			
ASUSTeK COMPUTER INC	Engineer: CH_LIN		
Size: C	Project Name: T13M		Rev: 1.1
Date: Friday, September 08, 2006	Sheet 11 of 65		



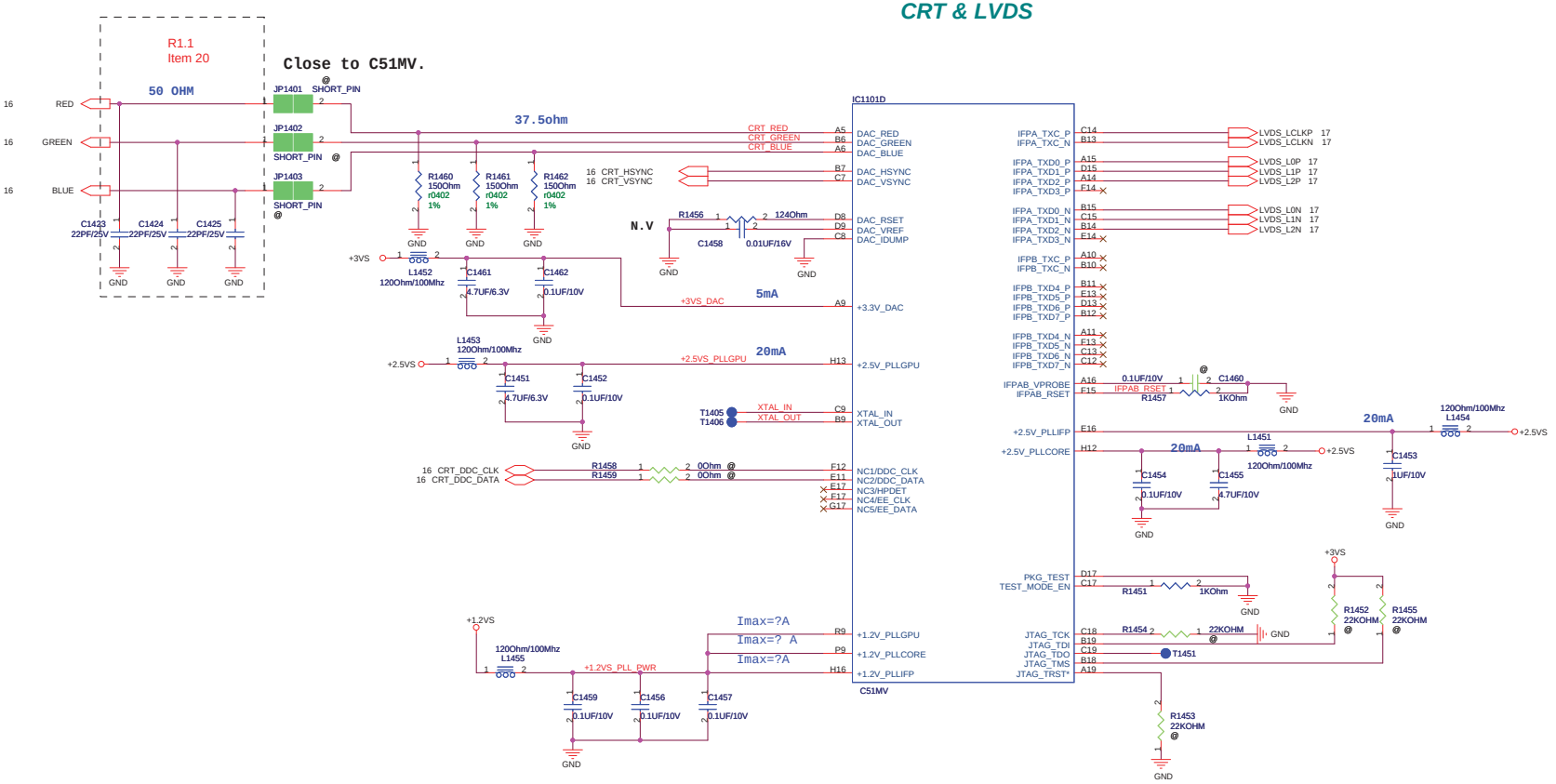
ASUSTeK COMPUTER INC	Title : C51MV HT TO MCP	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 12 of 65	

PCIE

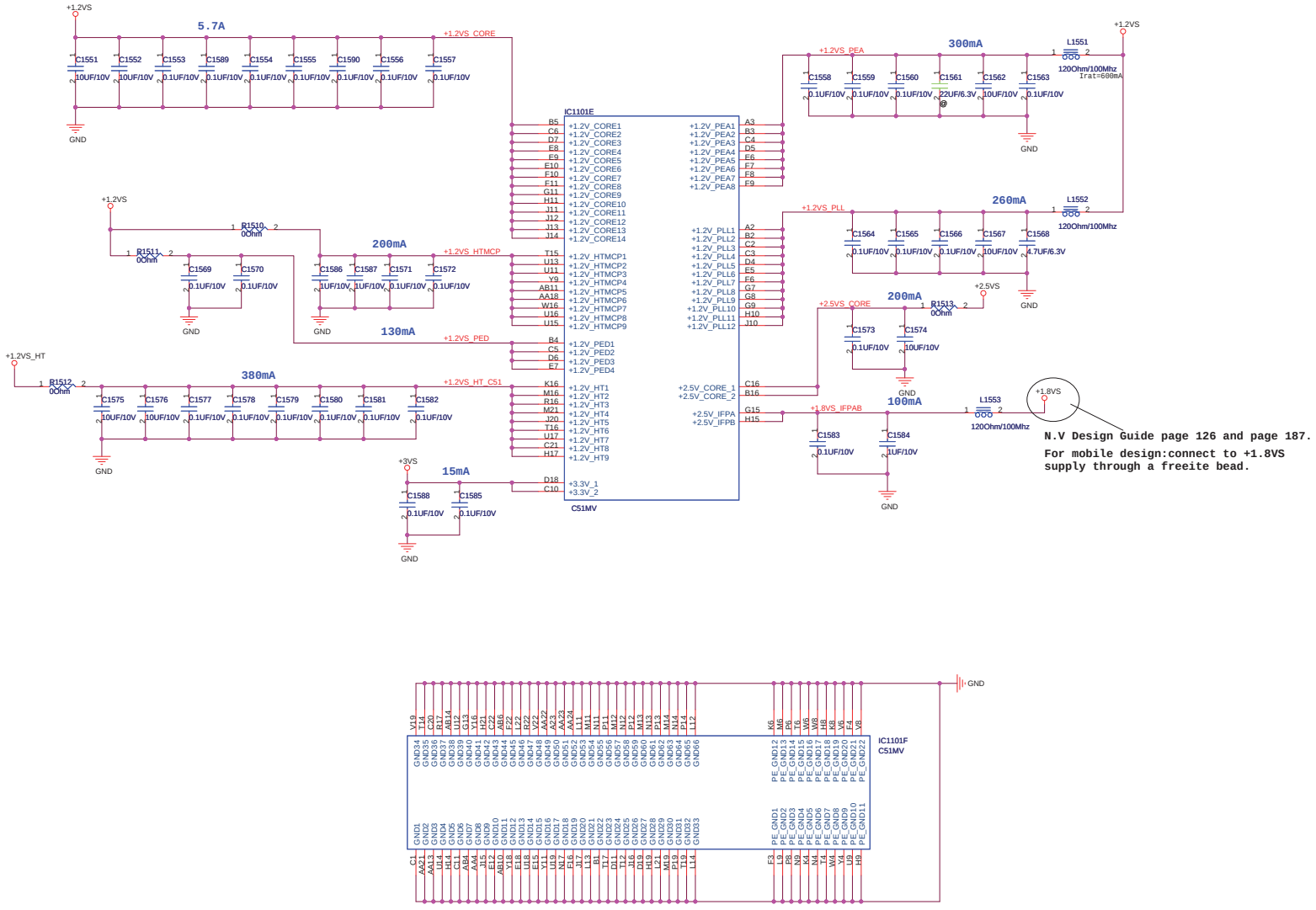


ASUSTeK COMPUTER INC	Title : C51MV PCIE	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 13 of 65	

CRT & LVDS

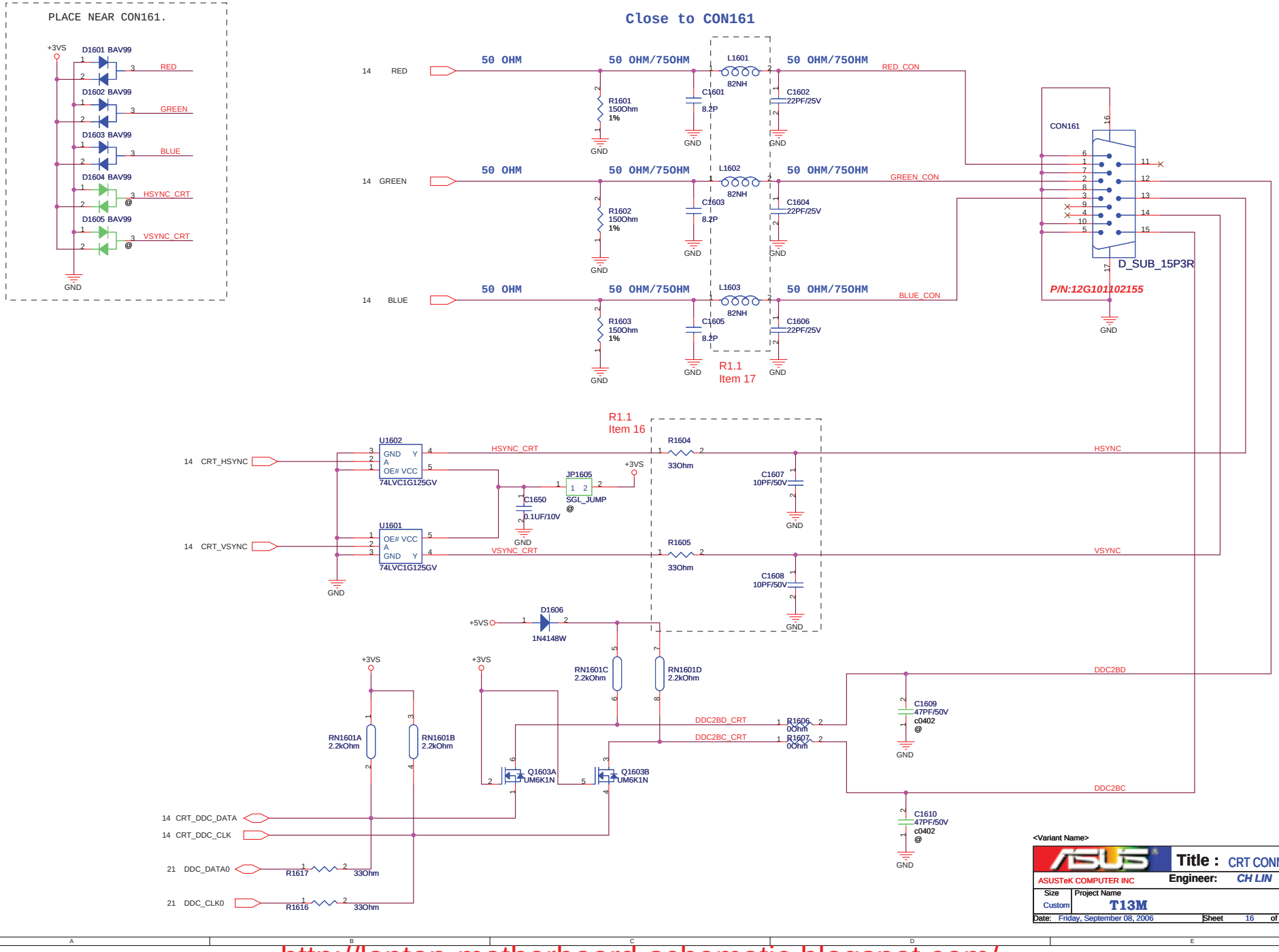


ASUSTeK COMPUTER INC	Title : C51MV VGA&LVDS	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 14 of 65	



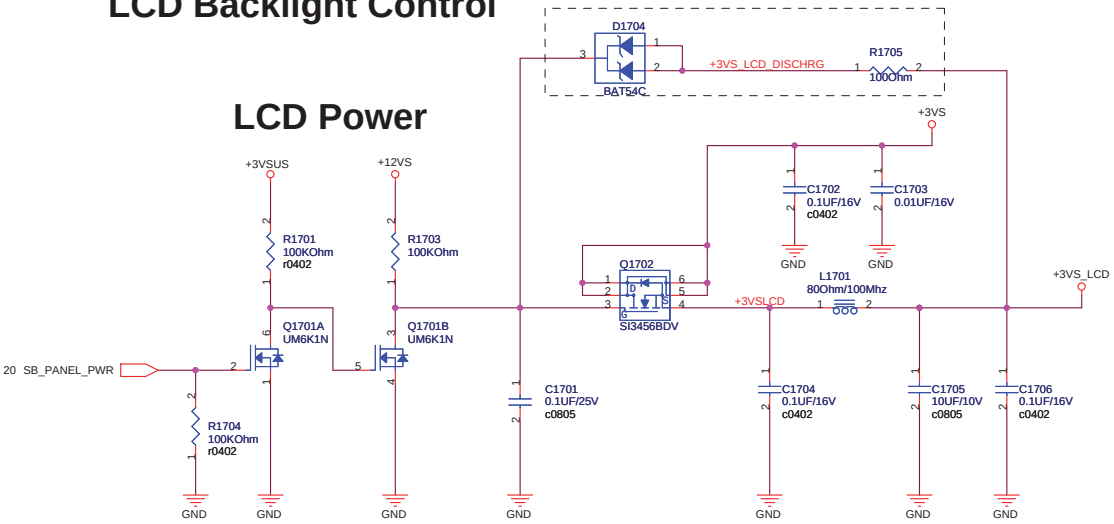
ASUSTeK COMPUTER INC	Title : C51MV POWER&GND		
	Engineer: CH_LIN		
Size: C	Project Name: T13M		Rev: 1.1
Date: Thursday, September 07, 2006	Sheet 15 of 65		

CRT



LCD Backlight Control

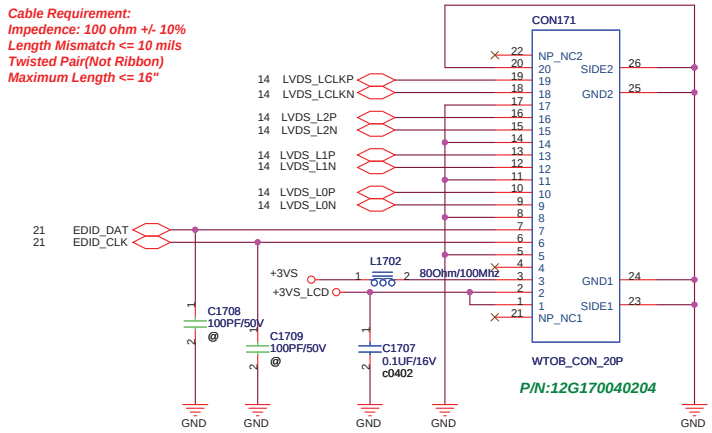
R1.1
Item 30



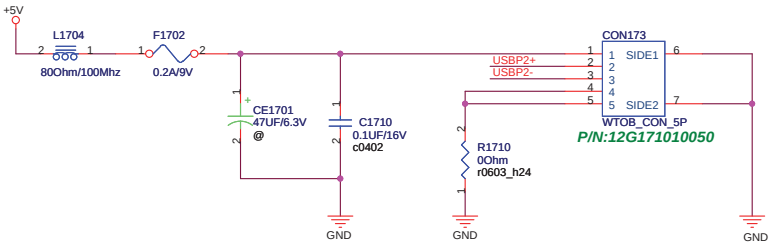
LCD Power

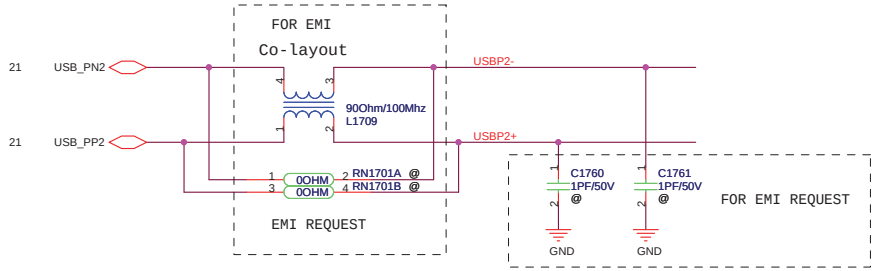
LCD LVDS Interface

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



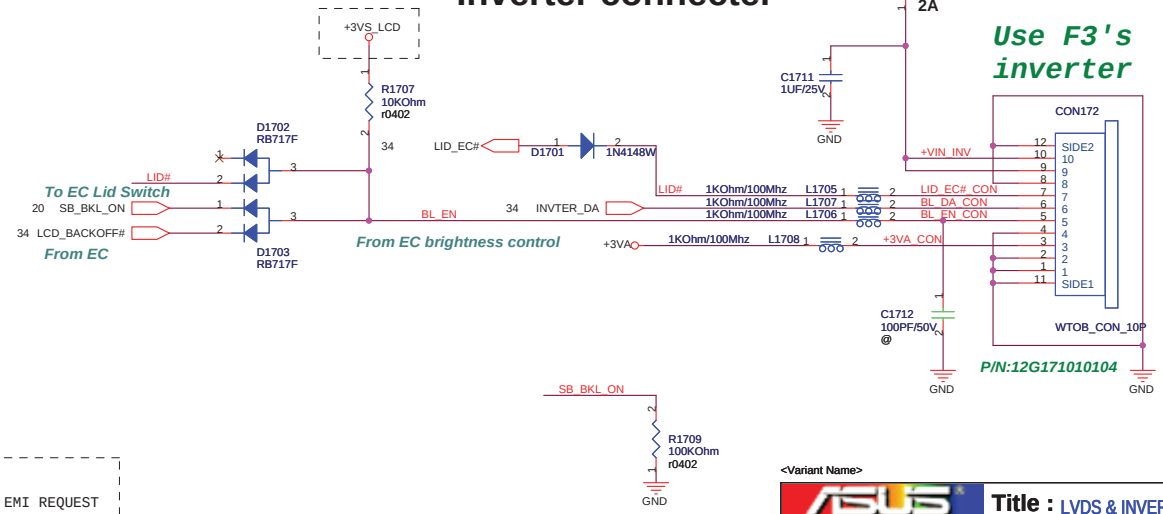
CCD connecter





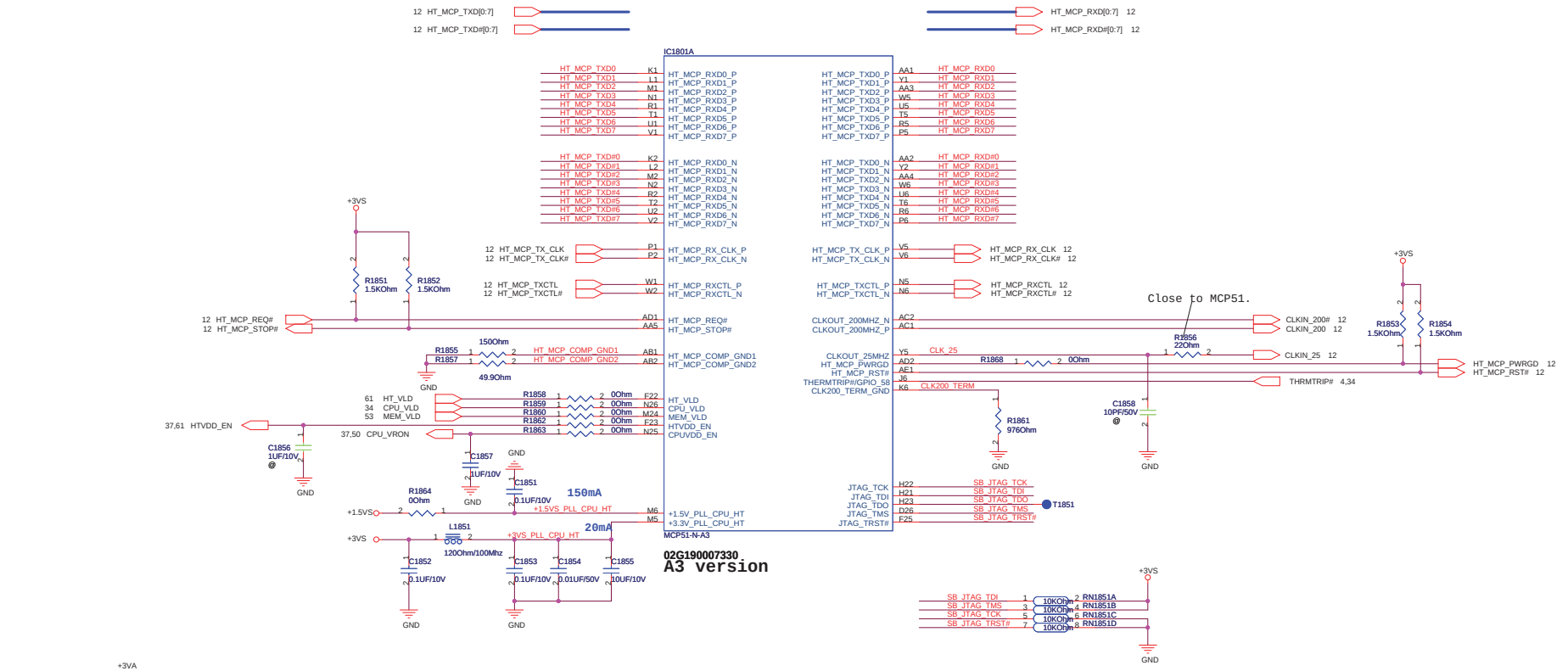
R1.1
Item 29

Inverter connecter

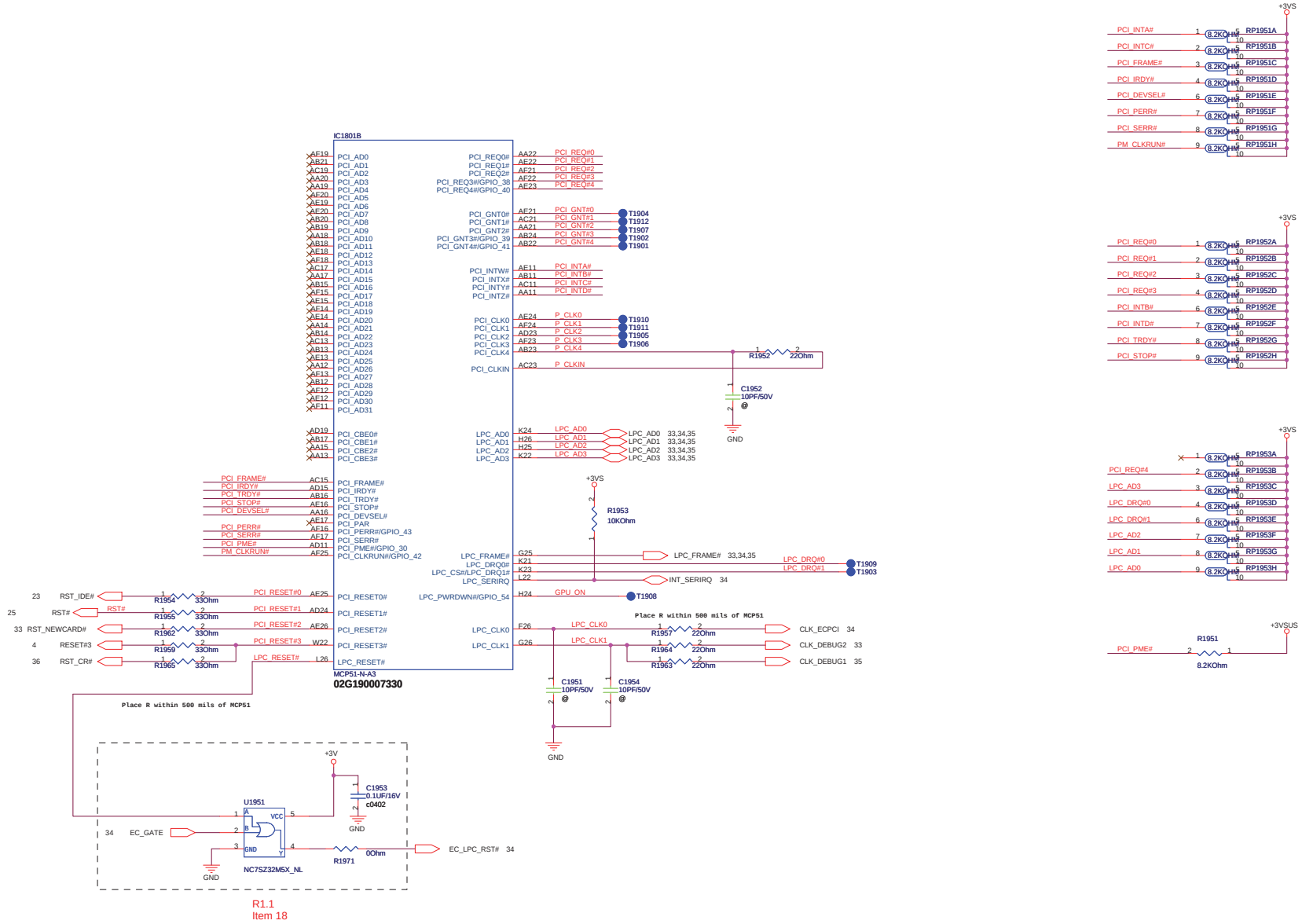


<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: CH LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 17 of 65	

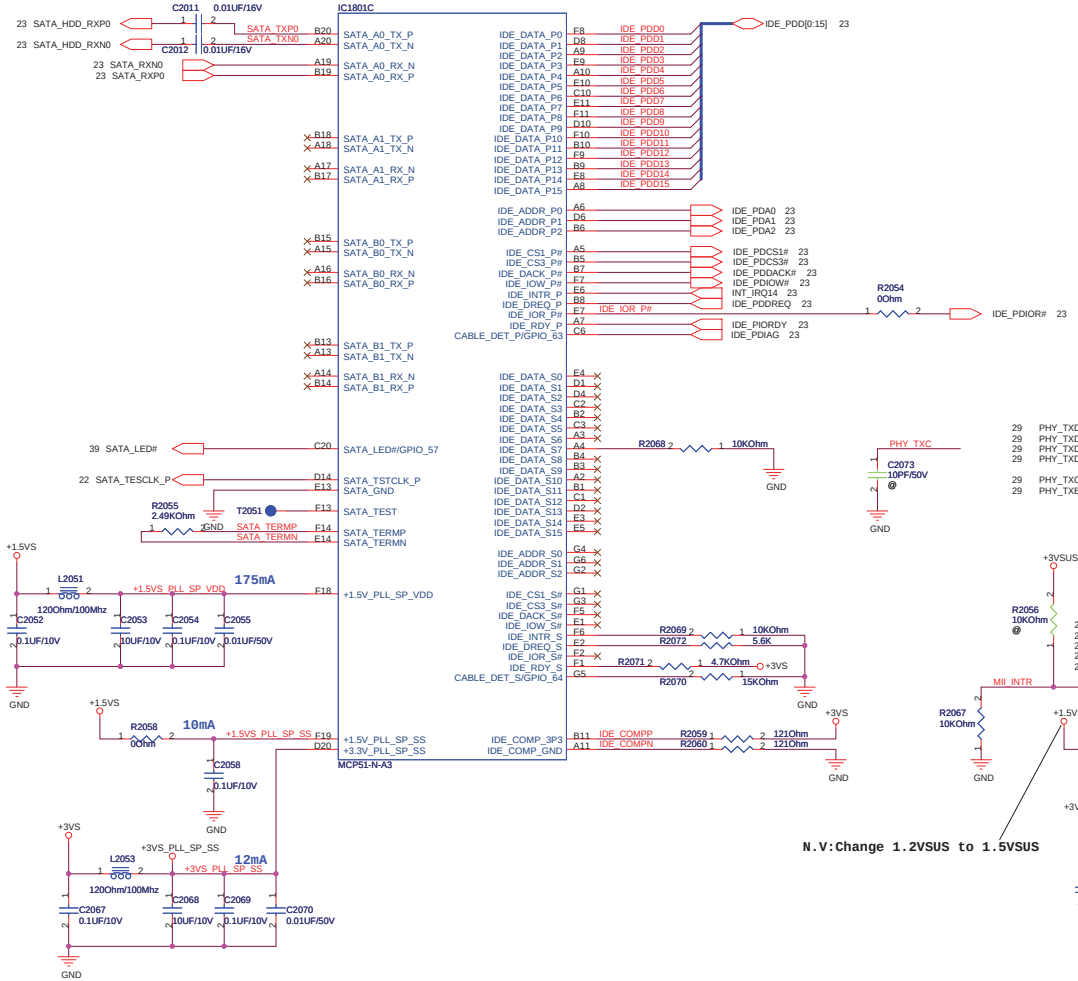


ASUSTeK COMPUTER INC	Title : MCP51_HT TO C51MV	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 18 of 65	

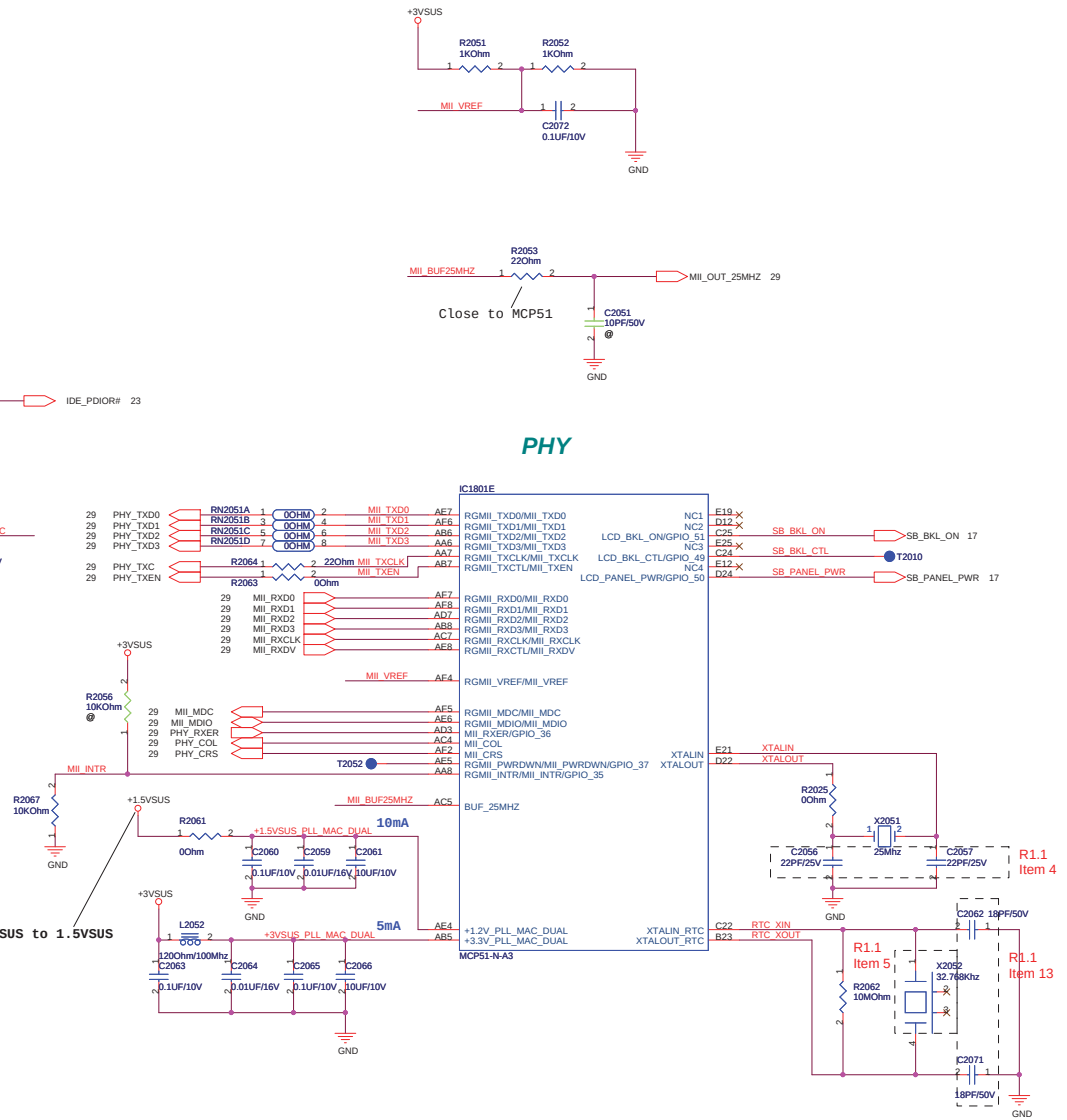


ASUSTeK COMPUTER INC	Title : MCP51_PCI I/F	
	Engineer: CH_LIN	
Size: C	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 19 of 65	

SATA & ODD

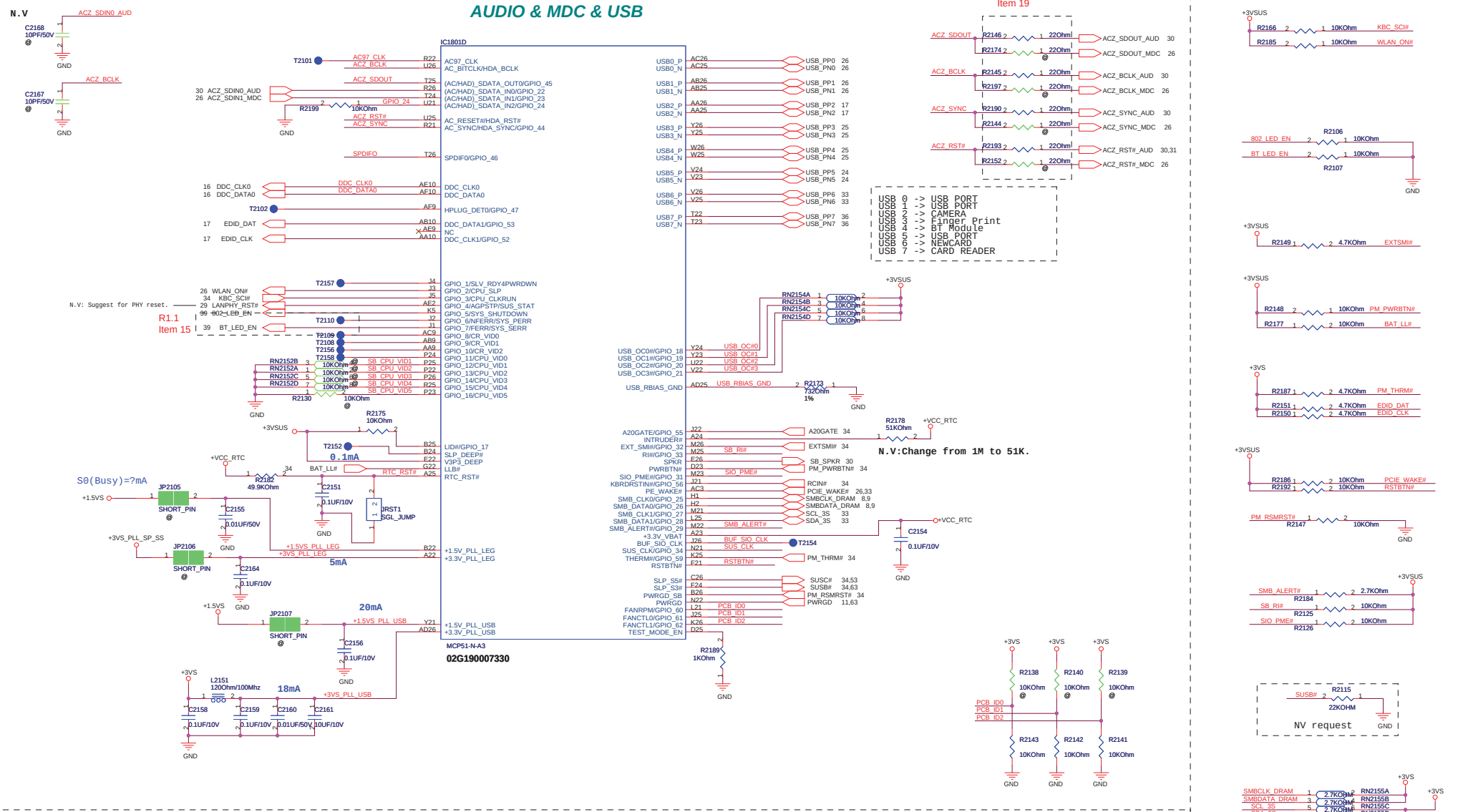


PHY

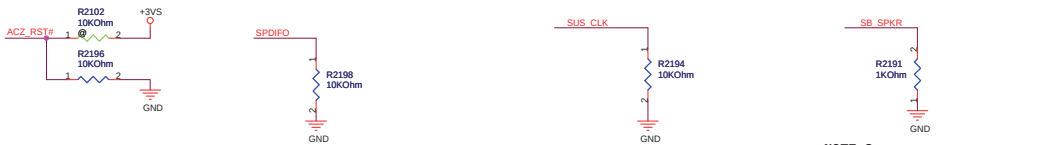


N.V:Change 1.2VSUS to 1.5VSUS

ASUSTeK COMPUTER INC	Title : MCP51_SATA&IDE&LAN		
	Engineer: CH_LIN		
Size: C	Project Name: T13M		Rev: 1.1
Date: Friday, September 08, 2006	Sheet 20 of 65		



Strap Option



ACZ_RST# select	
0	MII(10/100M) *
1	RGMII(1000/100/10M)

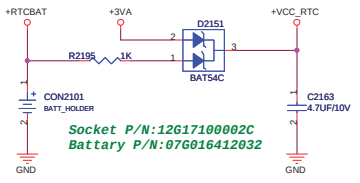
BUF_SIO_CLK select	
0	14.31818 MHz *
1	24 MHz

MCP51 master/slave mode	
0	normal *
1	slave mode

Boot mode select	
0	User Mode *
1	Safe Mode

NOTE 3

RTC BATTERY



Socket P/N:12G17100002C
Battary P/N:07G016412032

+VCC_RTC
S0(Busy)~S1=5mA
S3~S5=0.2mA
G3=0.1mA

N.V:Normal 8uA arround.Max:80uA~160uA arround

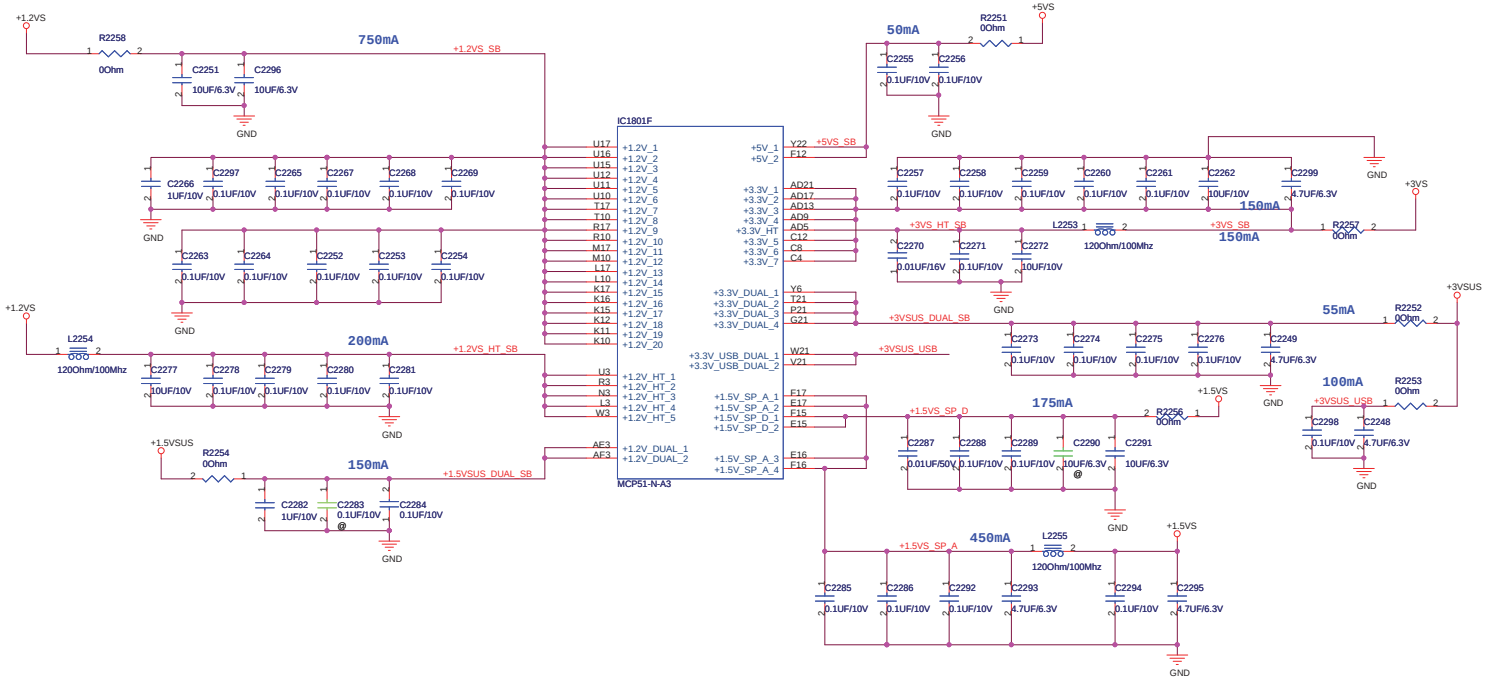
ASUSTeK COMPUTER INC

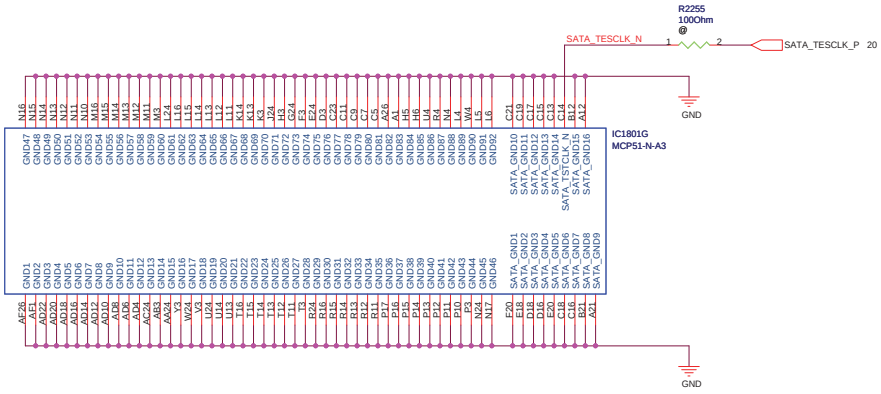
Title : MCP51_USB&GPIO&MISC

Engineer: CH_LIN

Size	Project Name	Rev
C	T13M	1.1

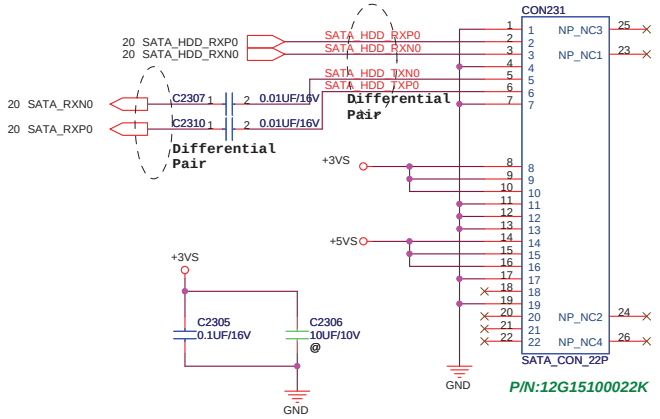
Date: Friday, September 08, 2006 Sheet 21 of 65

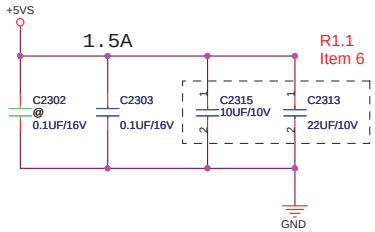




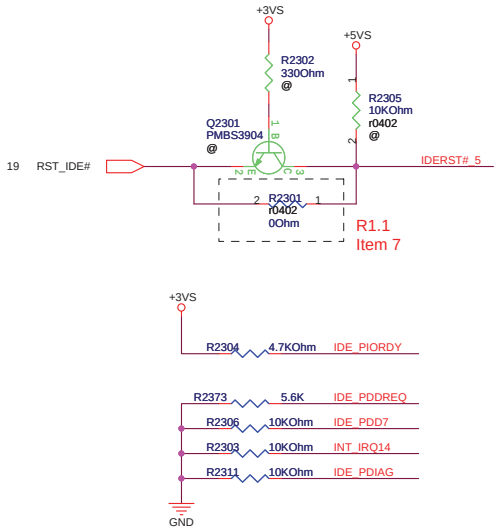
ASUSTeK COMPUTER INC	Title : MCP51_POWER&GND		
	Engineer: CH_LIN		
Size: C	Project Name: T13M		Rev: 1.1
Date: Friday, September 08, 2006	Sheet 22 of 65		

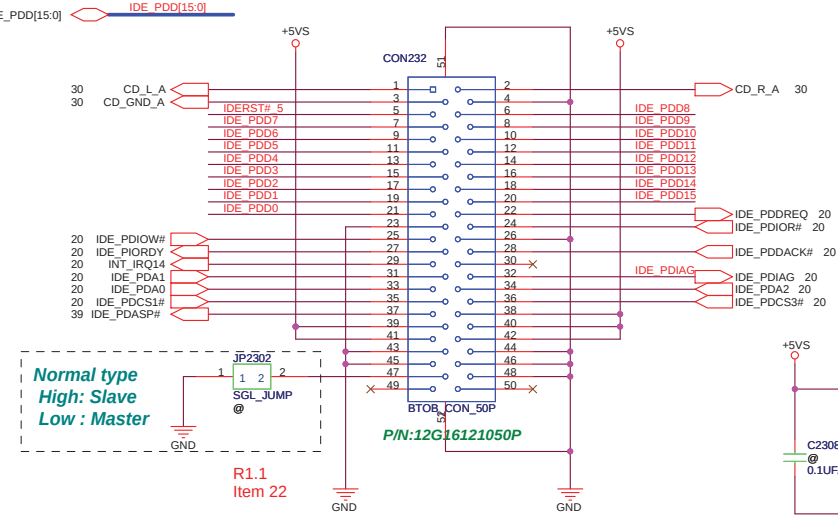
SATA HDD CON

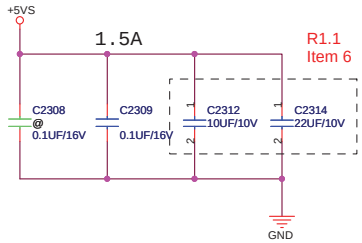




PATA ODD CON

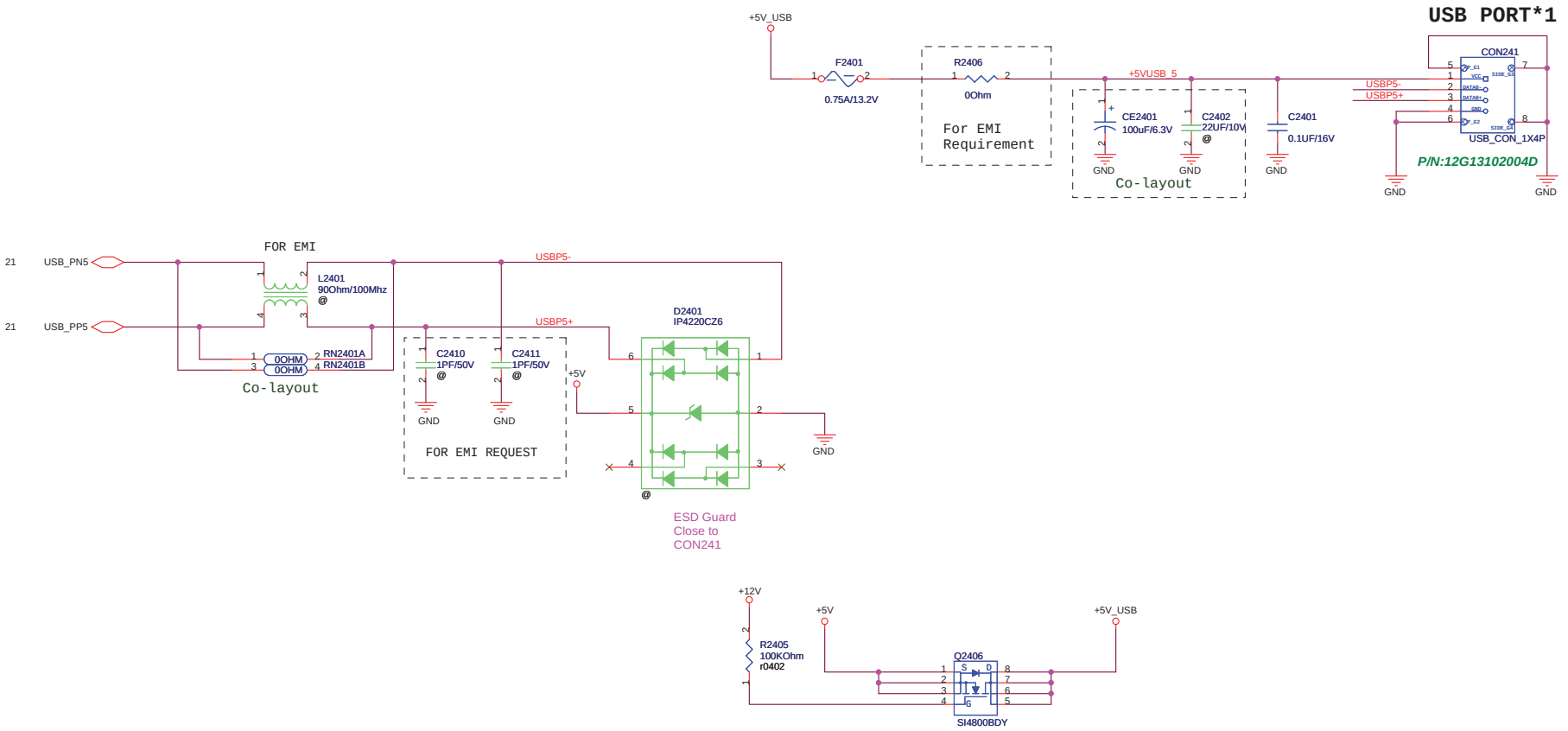






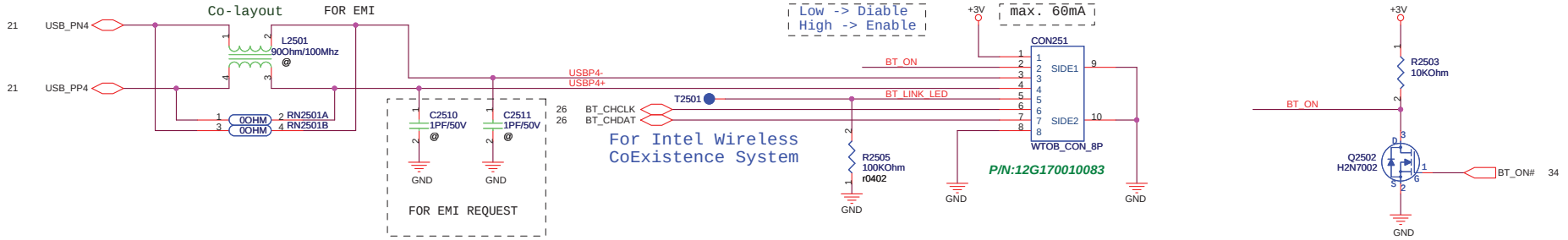
<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & ODD	
	Engineer: CH LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 23 of 65	

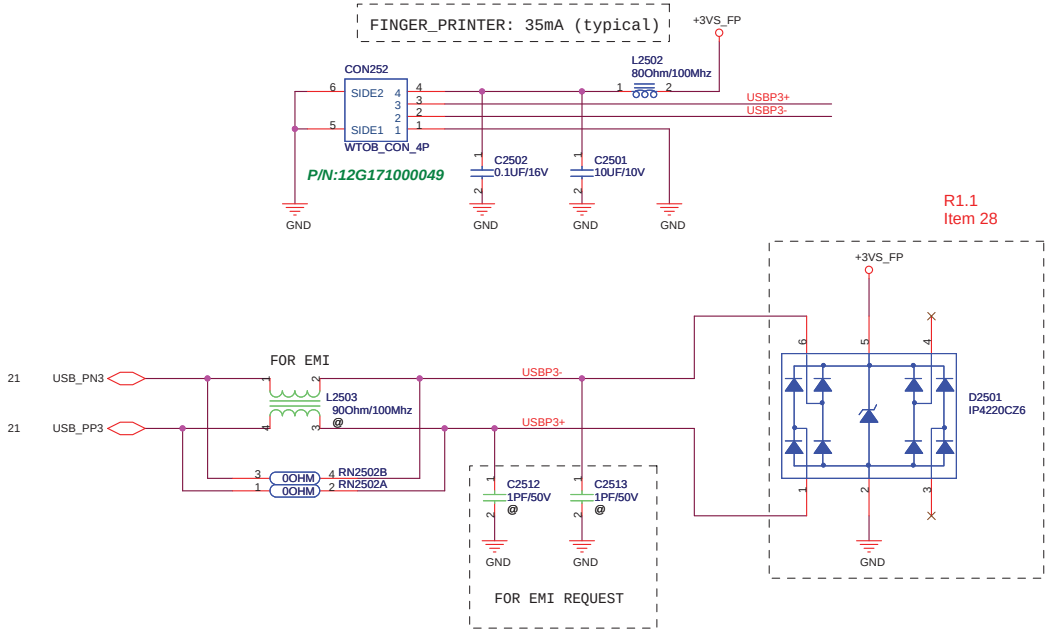


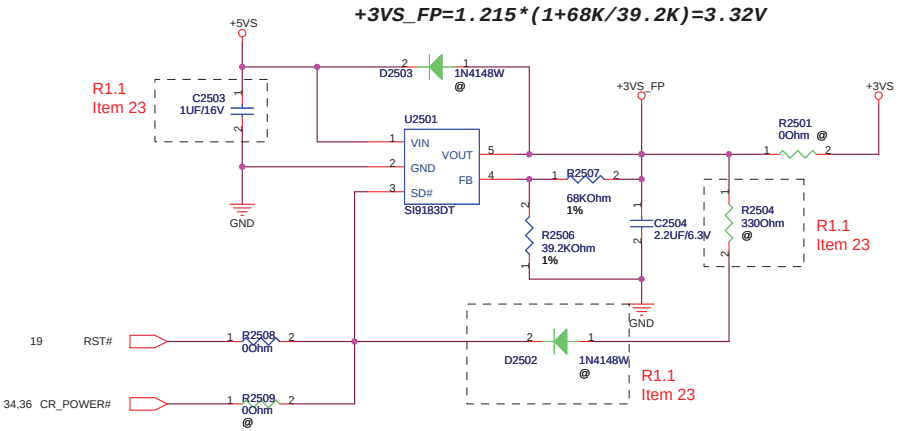
<Variant Name>

ASUSTeK COMPUTER INC	Title : USB PORT	
	Engineer: CH_LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 24 of 65	



Finger Printer





<Variant Name>

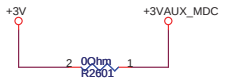
ASUSTeK COMPUTER INC	Title : BT & FP	
	Engineer: CH LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 25 of 65	

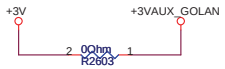
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

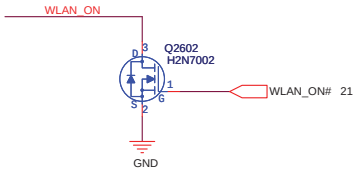
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA





Intel SPEC(18780):Internal
Pull UP 110Kohm



P/N:12G061200504

<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer: CH LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 26 of 65	

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 27 of 65

<Variant Name>

Title : EMPTY

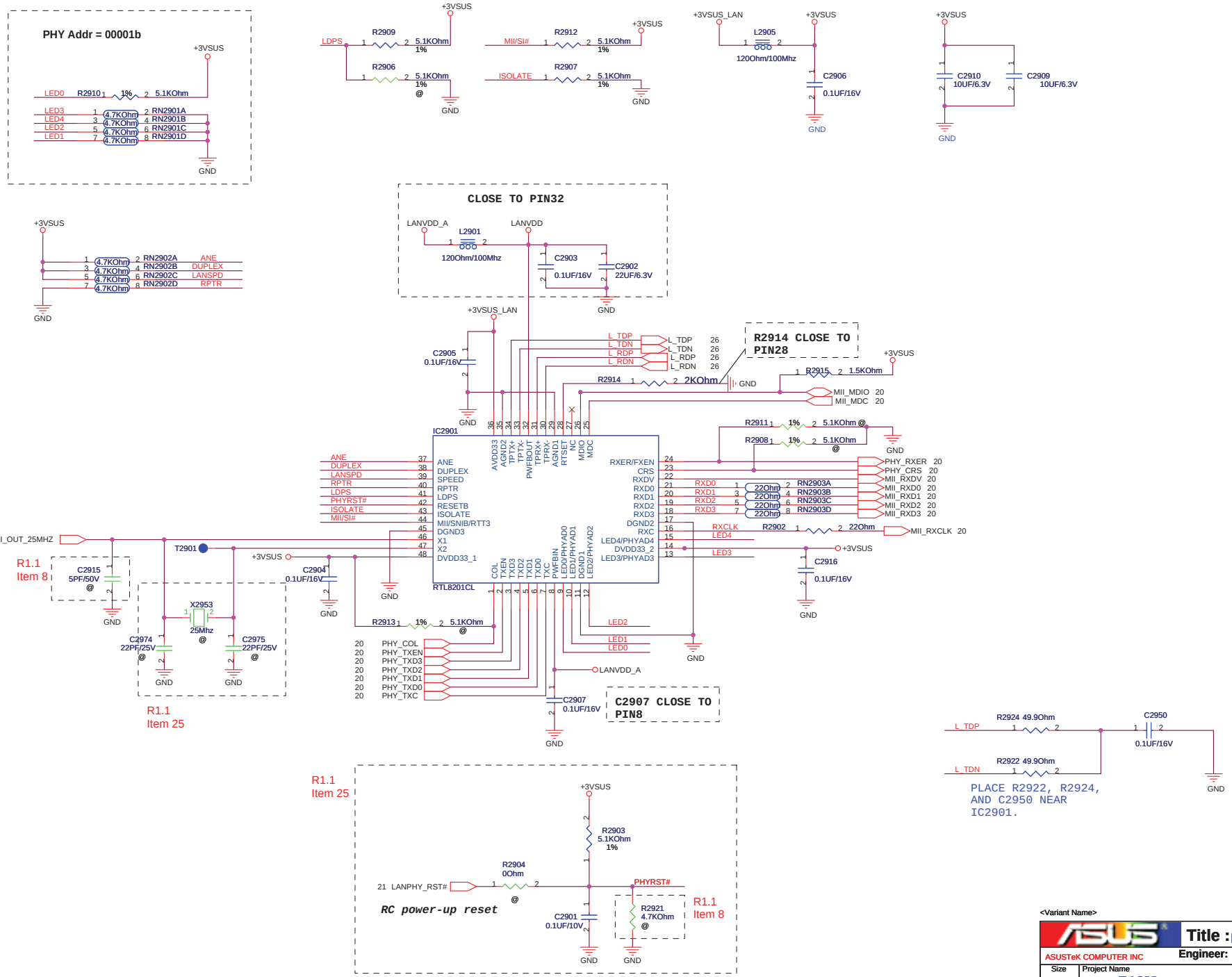
ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
C	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 28 of 65

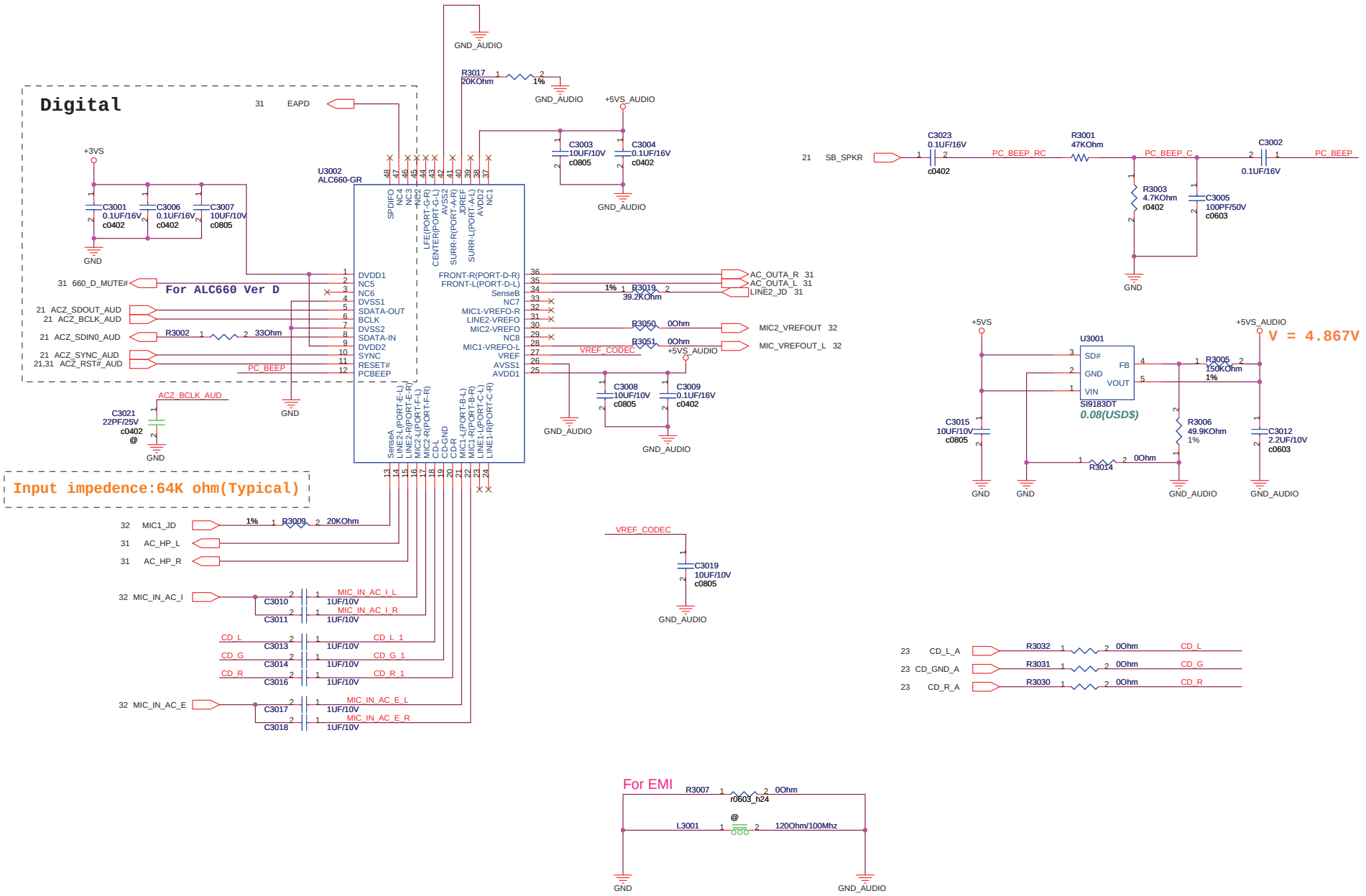
PHY



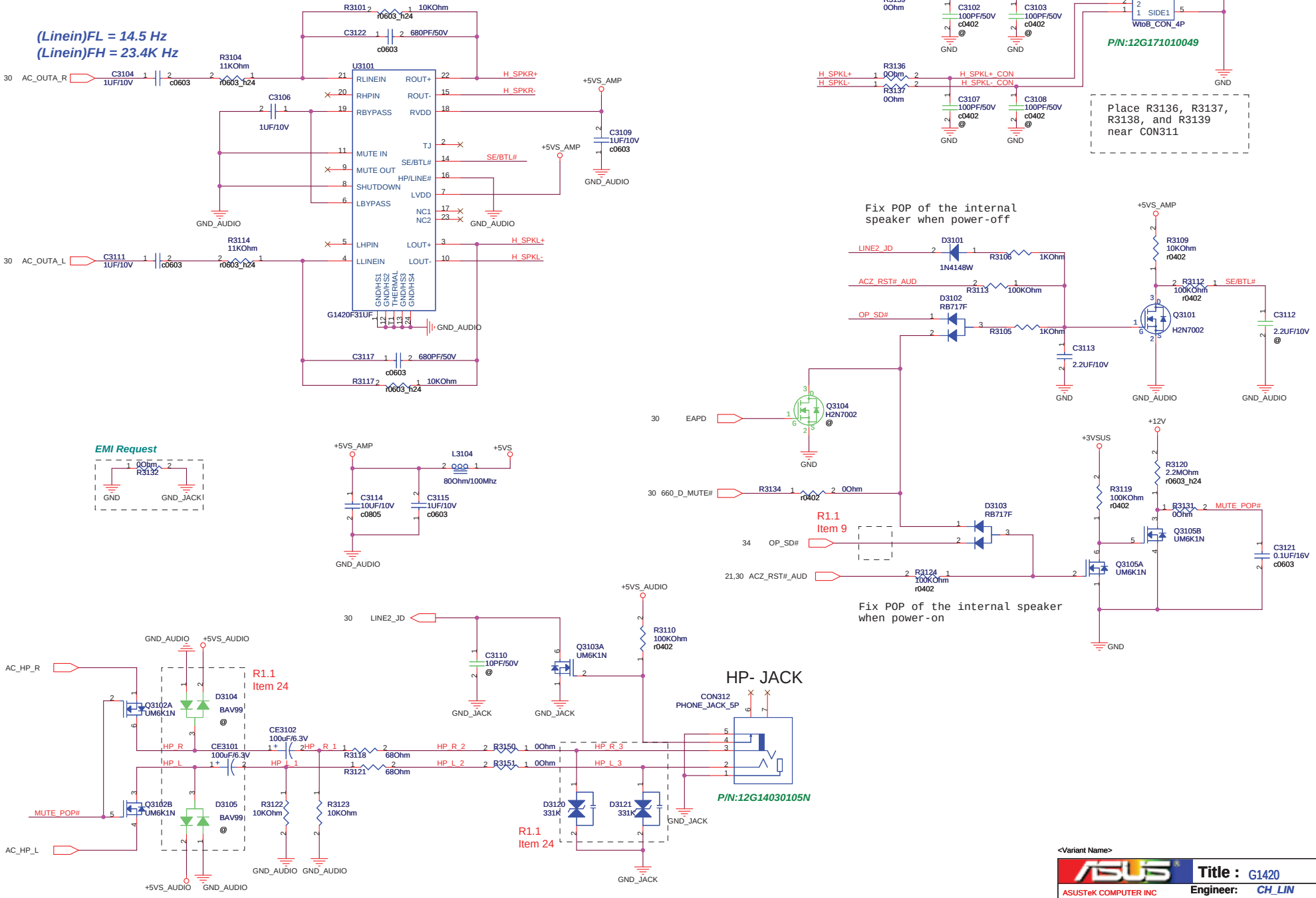
<Variant Name>

ASUSTeK COMPUTER INC	Title : PHY RTL8201CL(10/100)	
	Engineer: CH_LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 29 of 65	

CODEC



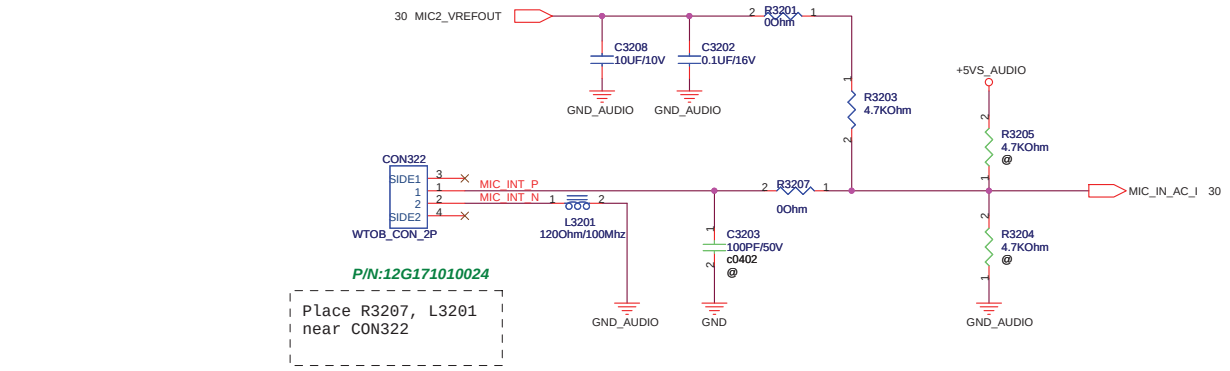
SPEAKER AMP

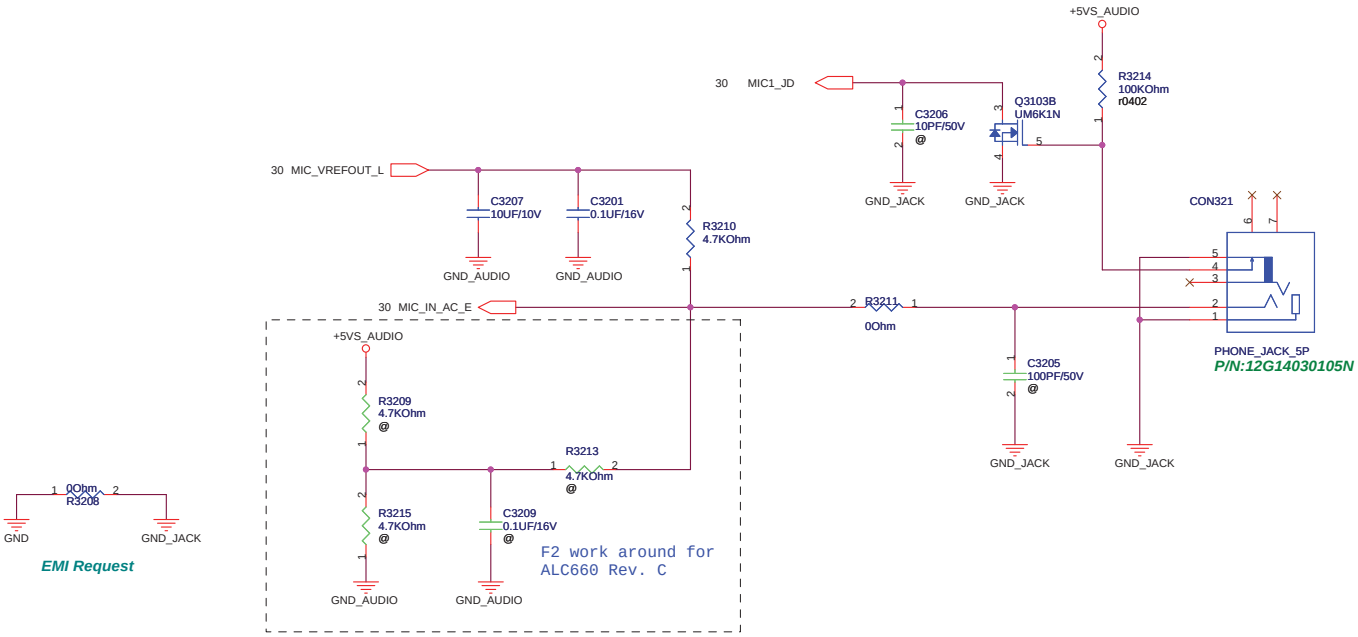


<Variant Name>

ASUSTeK COMPUTER INC	Title : G1420	
	Engineer: CH_LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 31 of 65	

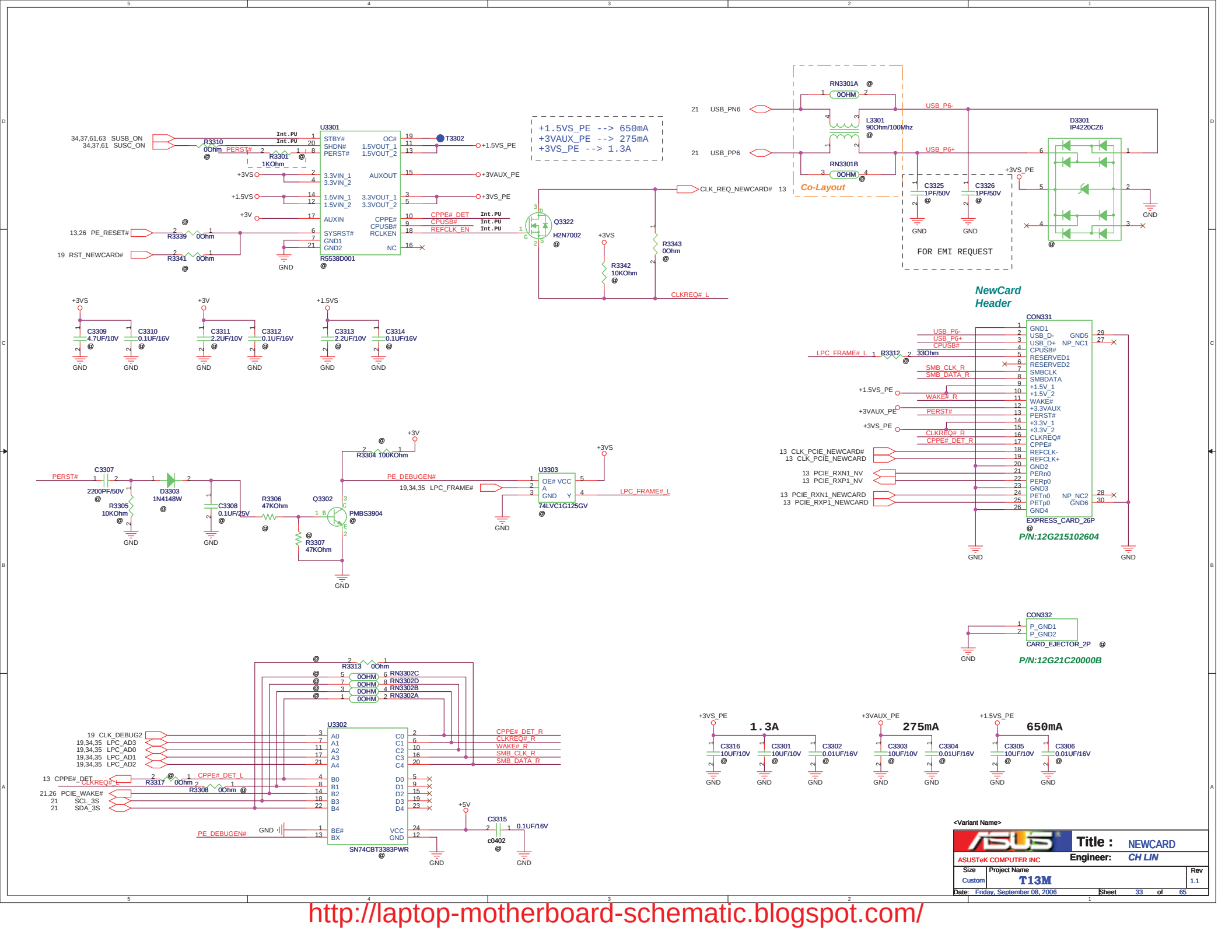
MIC



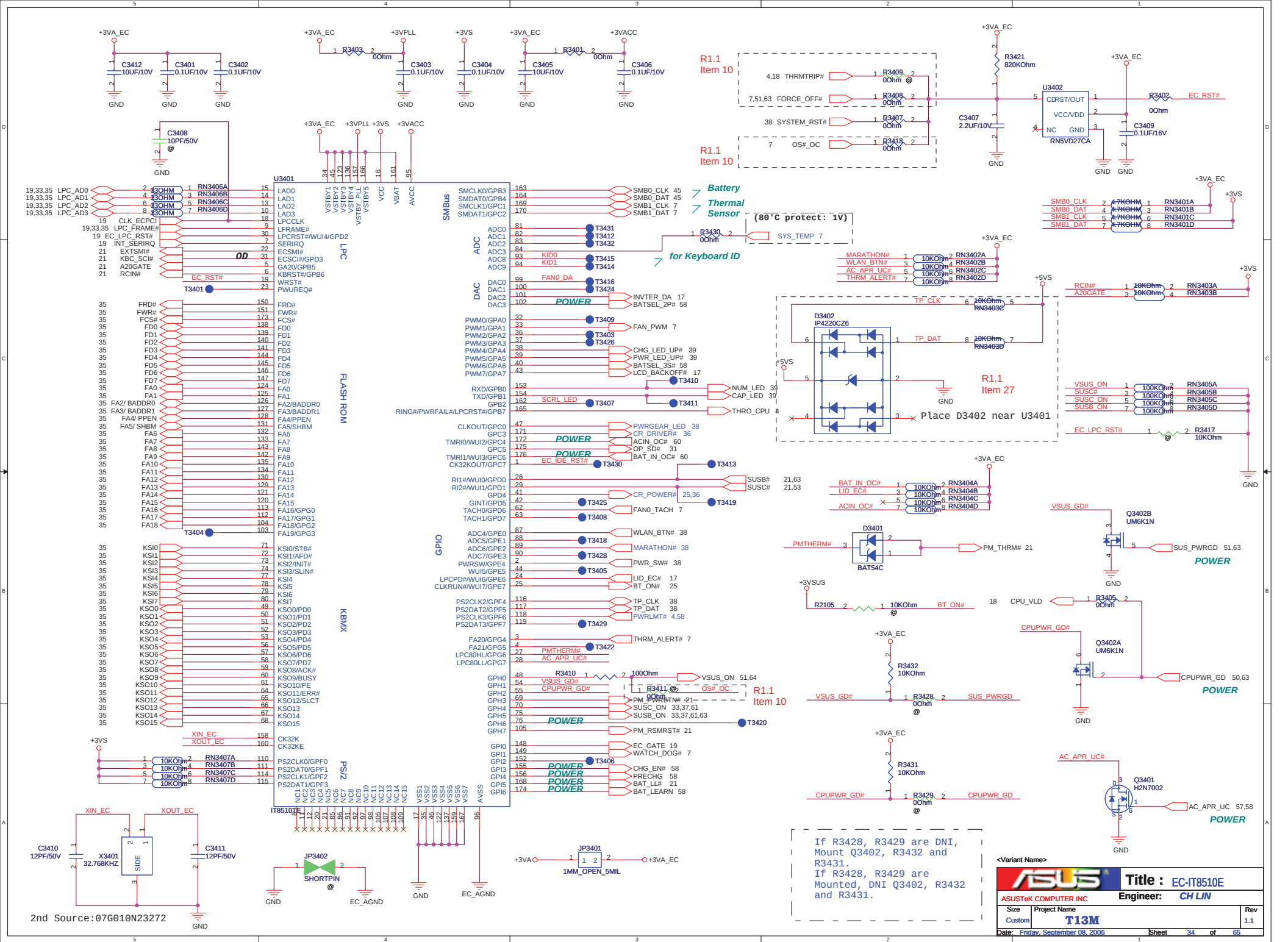


<Variant Name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: CH LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 32 of 65	



Variant Name	
Title	NEWCARD
Company	ASUSTeK COMPUTER INC
Engineer	CH LIN
Size	Custom
Project Name	T13M
Rev	1.1
Date	Friday, September 08, 2006
Sheet	33 of 65



EC Hardware Strapping

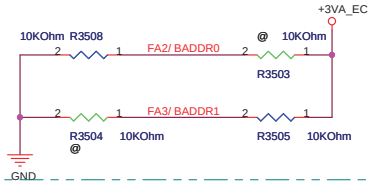
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

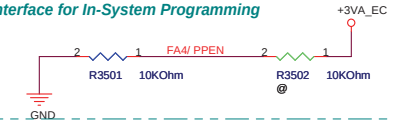


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

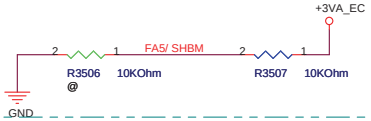
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



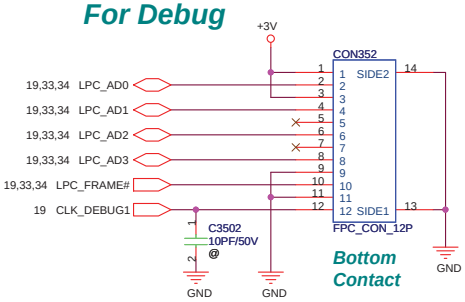
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



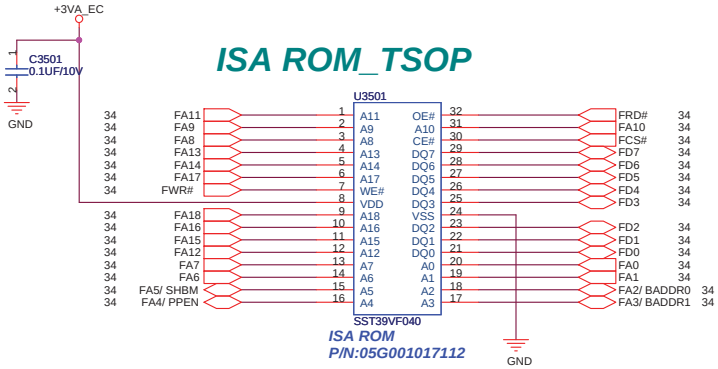
For Debug



Bottom Contact

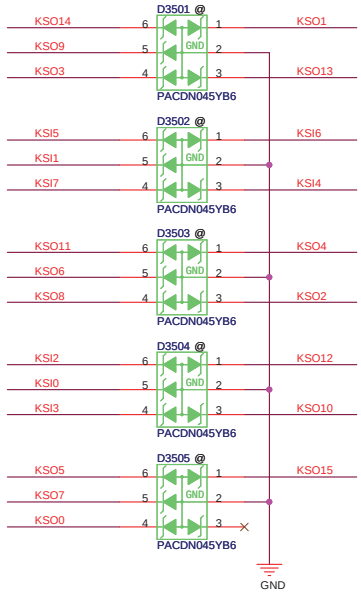
P/N:12G183301208

ISA ROM_TSOP

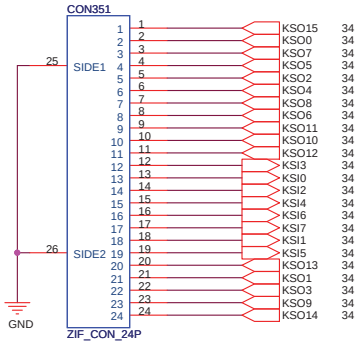


ISA ROM

P/N:05G001017112



For Keyboard

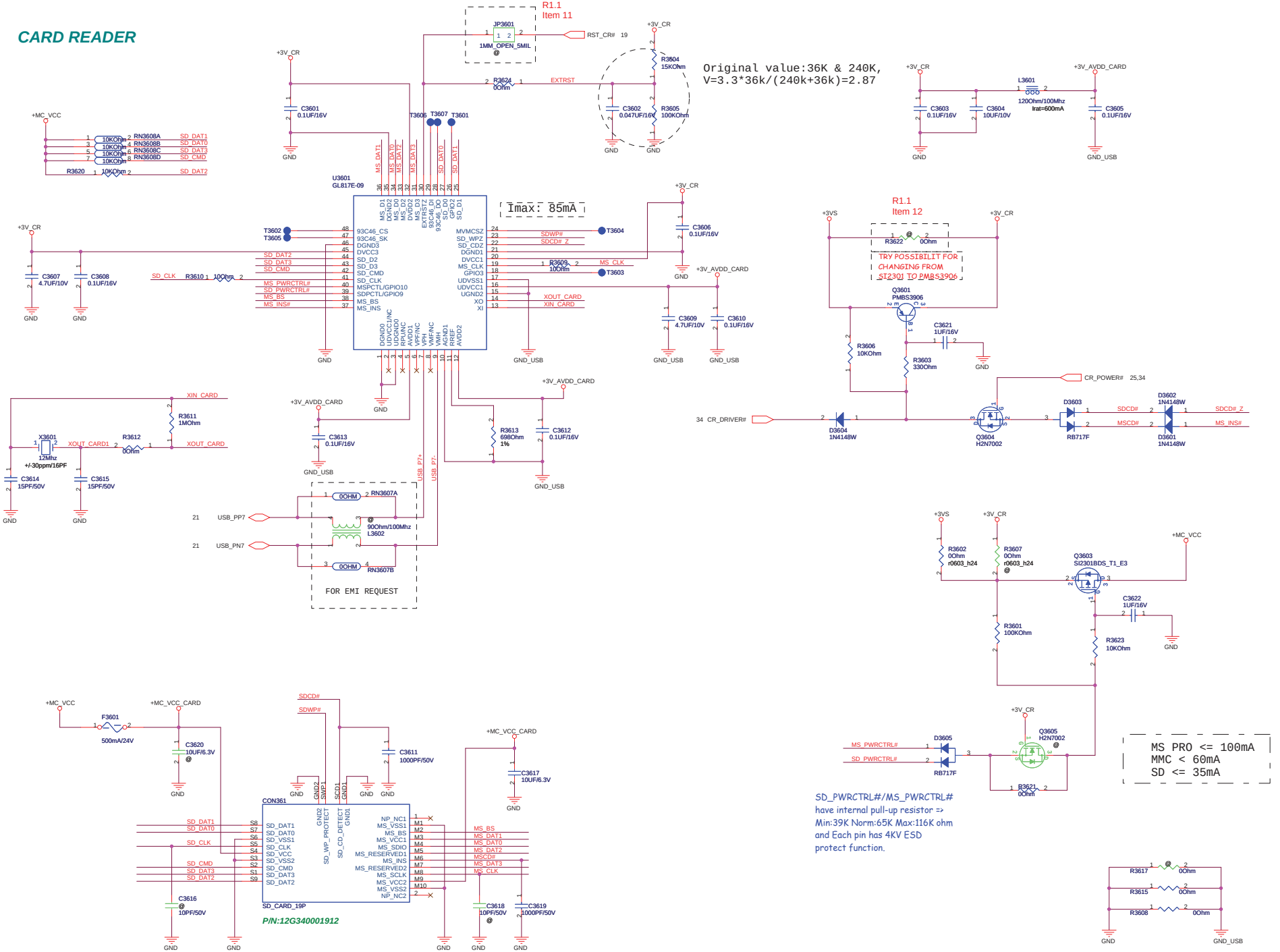


P/N:12G182402404

<Variant Name>

Title :	ISA_ROM&KB conn
ASUSTeK COMPUTER INC	Engineer: CH LIN
Size: Custom	Project Name: T13M
Rev: 1.1	
Date: Friday, September 08, 2006	Sheet 35 of 65

CARD READER



<Variant Name>

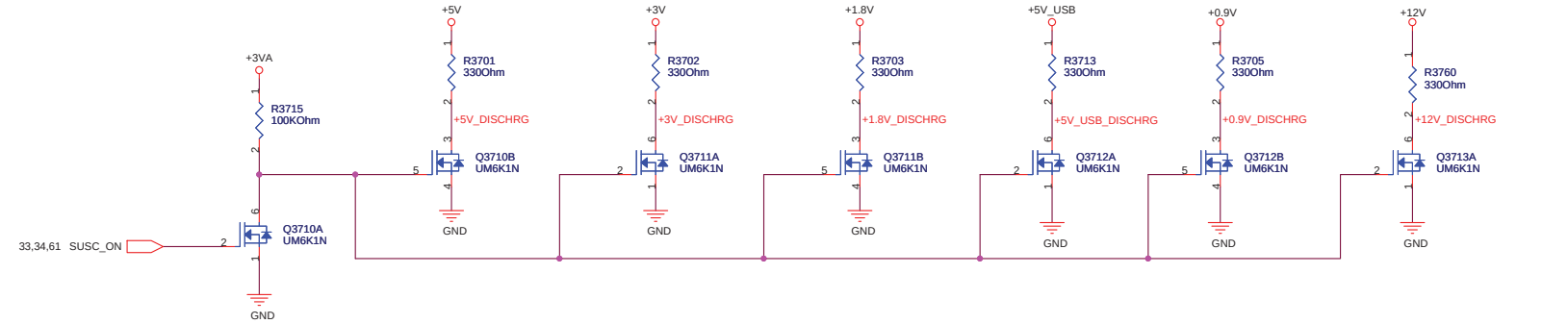
Title : 3IN1 CARD-READER

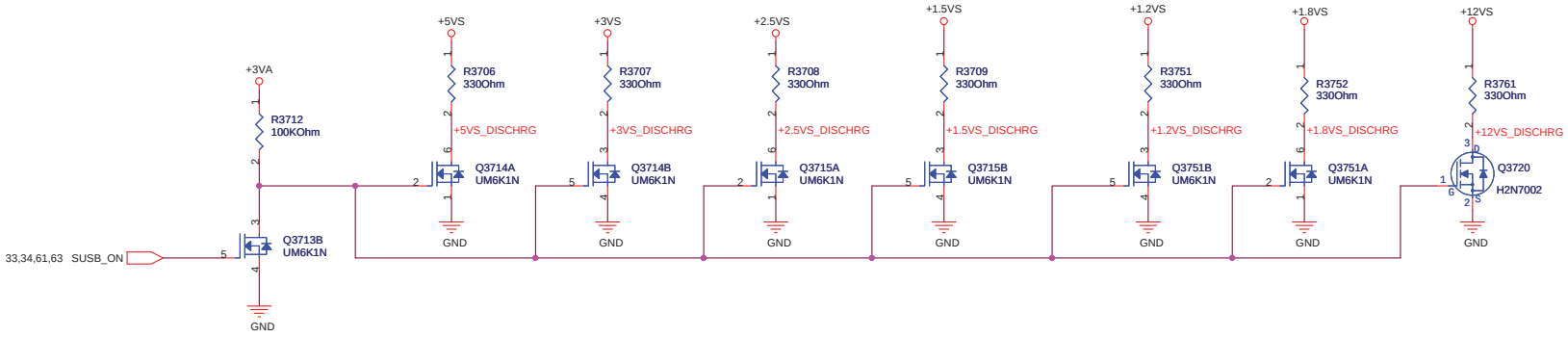
ASUSTeK COMPUTER INC

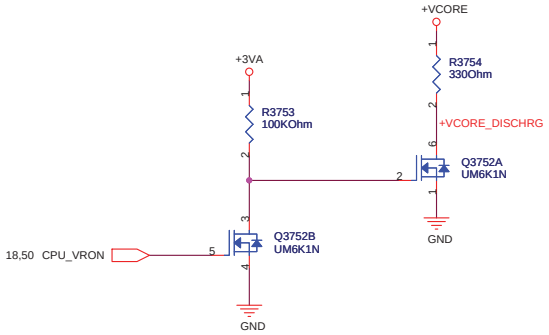
Engineer: CH LIN

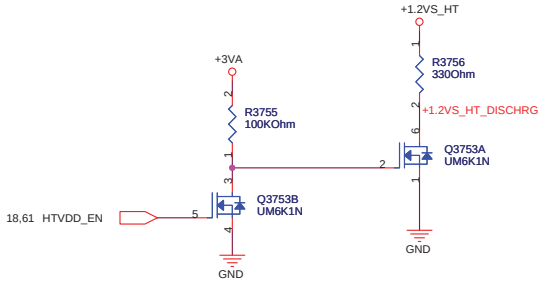
Size	Project Name	Rev
C	T13M	1.1

Date: Friday, September 08, 2006 Sheet 36 of 65









<Variant Name>

ASUSTeK COMPUTER INC

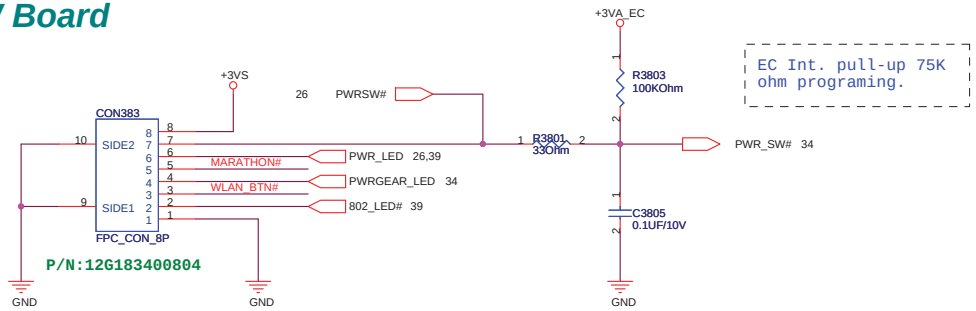
Title : DISCHARGE

Engineer: CH_LIN

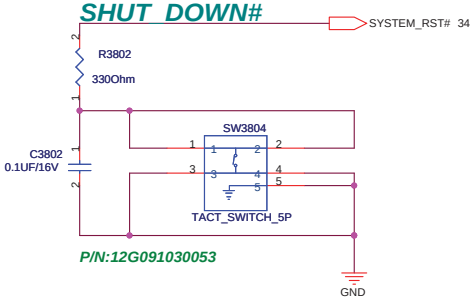
Size	Project Name	Rev
Custom	T13M	1.1

Date: Friday, September 08, 2006 Sheet 37 of 65

FFC CONNECTER for T13Mv SW Board

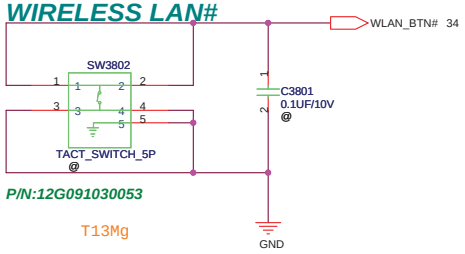


SHUT_DOWN#

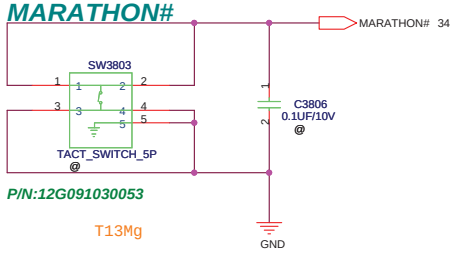


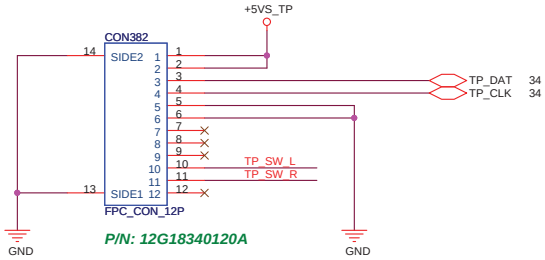
INSTANT KEY

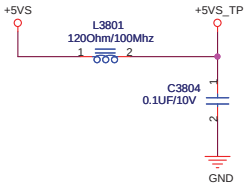
WIRELESS LAN#



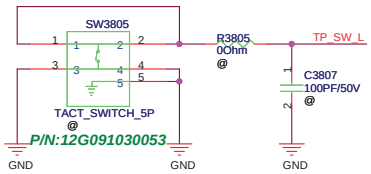
MARATHON#

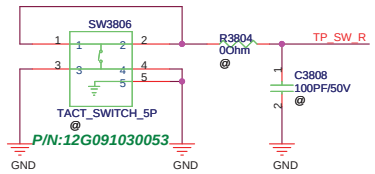






Select Button for T13Mg



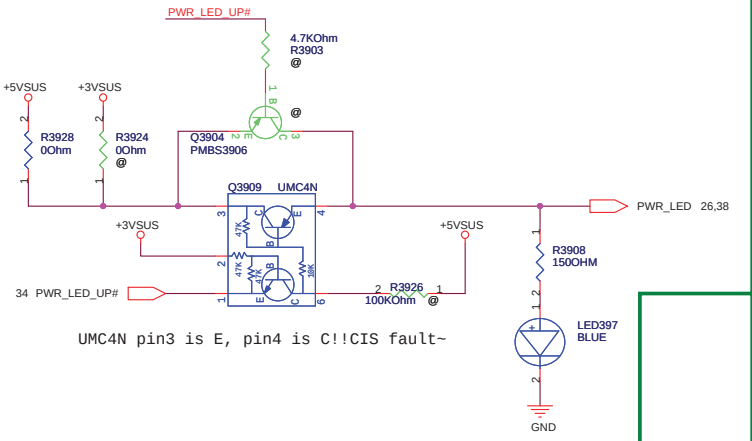


<Variant Name>

ASUSTeK COMPUTER INC	Title : Key & FFC CONN	
	Engineer: CH LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 38 of 65	

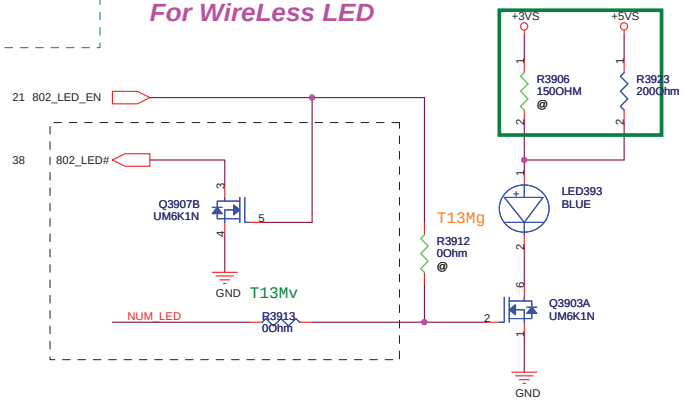
For T13Fg: Change LED397, LED393, LED394, LED391, LED395, LED396 to 07G015700771 *Green
,change R3908 to 10G213101003010 *100 ohm, and change LED392 to 07G015700294* Orange.
Mount R3924, R3903, Q3904, Q3902, R3902, R3905, R3906, R3912, R3909, R3918, R3907, R3915,
R3910
DNI R3928, Q3909, R3923, R3913, Q3908, R3919, R3921, R3917, R3922, R3920, R3916

For POWER LED

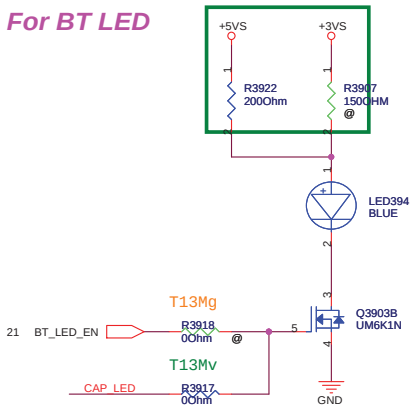


UMC4N pin3 is E, pin4 is C!!CIS fault~

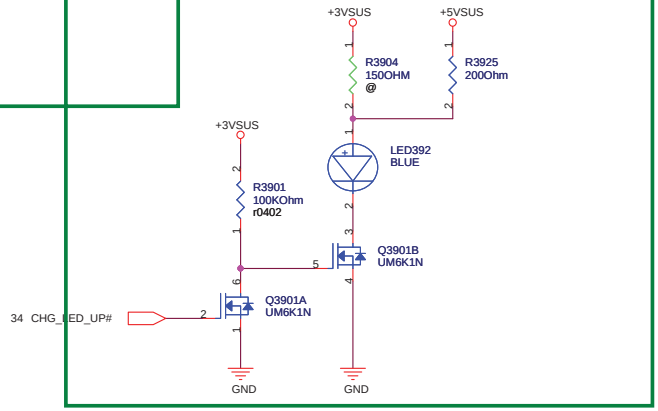
For WireLess LED



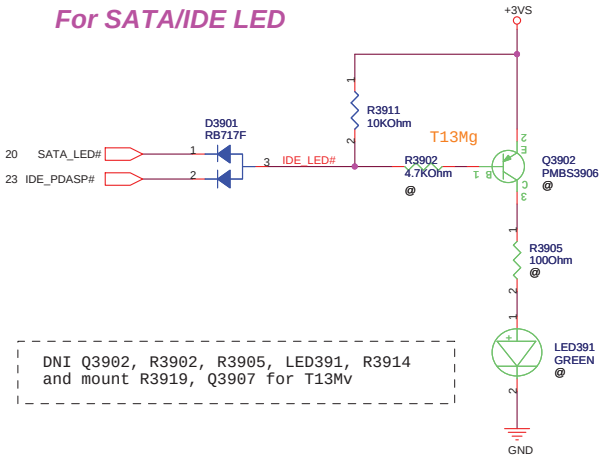
For BT LED



For BATTERY LED

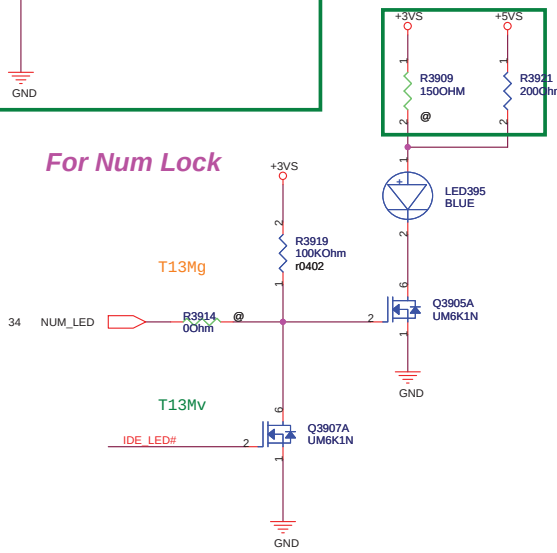


For SATA/IDE LED

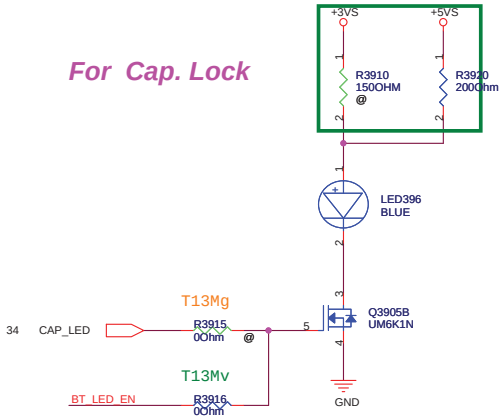


DNI Q3902, R3902, R3905, LED391, R3914
and mount R3919, Q3907 for T13Mv

For Num Lock



For Cap. Lock



<Variant Name>

ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer: CH_LIN	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 39 of 65	

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 40 of 65

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 41 of 65

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 42 of 65

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 43 of 65

<Variant Name>

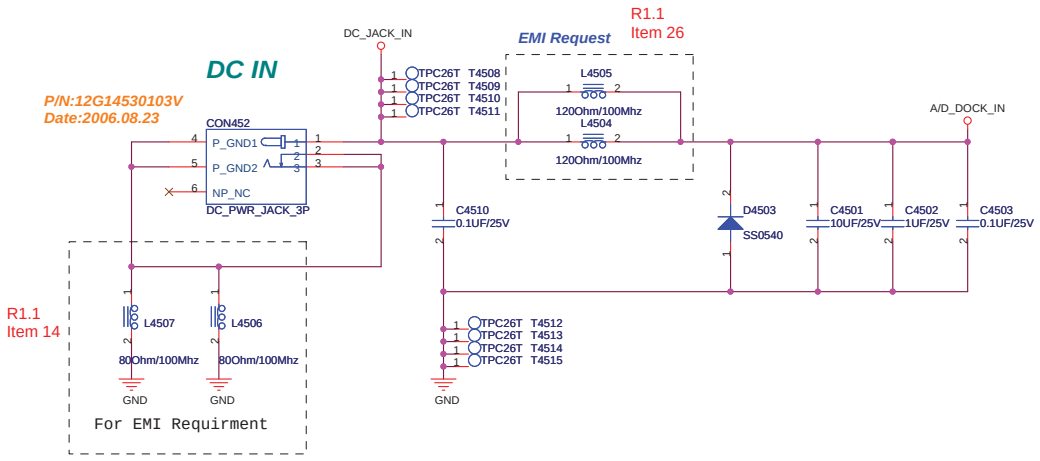
ASUSTeK COMPUTER INC

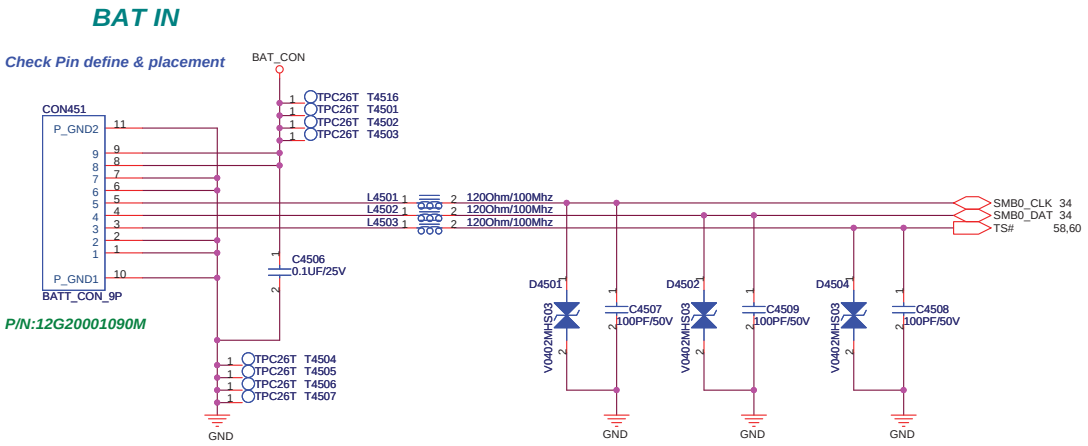
Title : EMPTY

Engineer: CH_Lin

Size	Project Name	Rev
C	T13M	1.1

Date: Friday, September 08, 2006 Sheet 44 of 65





<Variant Name>

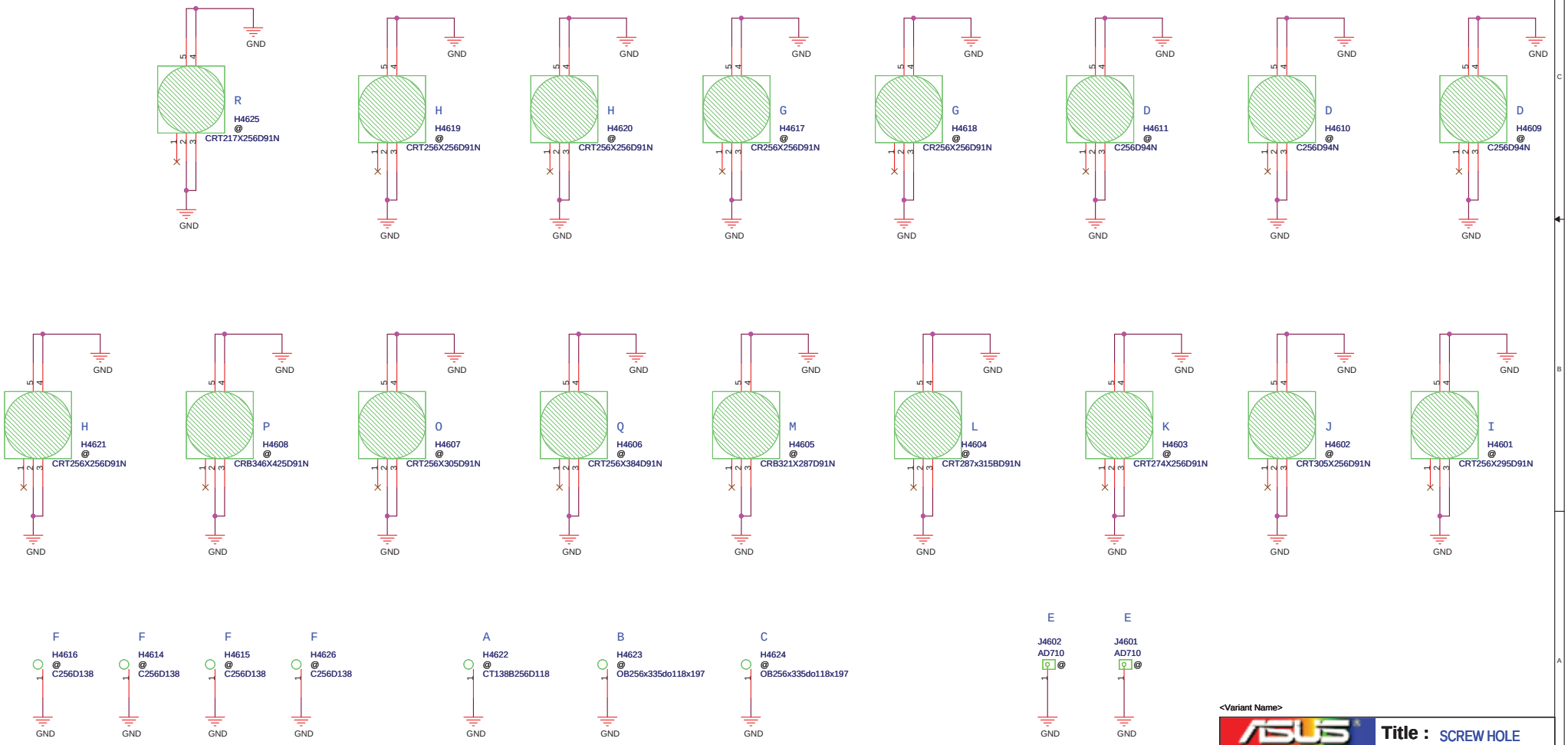
Title : BAT&Adapter conn

ASUSTeK COMPUTER INC

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Friday, September 08, 2006 Sheet 45 of 65



<Variant Name>

ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer: CH LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 46 of 65

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	I
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	CR_DRIVER#	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	LPC_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	CR_POWER#	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	
88	ADC5/GPE1	N/A	
89	ADC6/GPE2	MARATHON#	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	
25	CLKRUN#/WUI7/GPE7	BT_ON#	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	
28	LPC80LL/GPG7	AC_APR_UC#	

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	N/A	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010010x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

NV MCP51

Pin		Use As	Signal Name	Power
GPIO 1	i	GPO		+3VS
GPIO 2	i	GPO	WLAN_ON#	+3VSUS
GPIO 3	i	GPI	KBC_SCI#	+3VSUS
GPIO 4	i	GPO	LANPHY_RST#	+3VSUS
GPIO 5	i	GPO	802_LED_EN	+3VSUS
GPIO 6	i	GPO	BT_LED_EN	+3VSUS
GPIO 7	i	GPO		+3VSUS
GPIO 8	i	GPO		+3VSUS
GPIO 9	i	GPO		+3VSUS
GPIO 10	i	GPO		+3VSUS
GPIO 11	i	GPO	MSK_PCIRST	+3VSUS
GPIO 12	i	GPO		+3VSUS
GPIO 13	i	GPO		+3VSUS
GPIO 14	i	GPO		+3VSUS
GPIO 15	i	GPO		+3VSUS
GPIO 16	i	GPO		+3VSUS
GPIO 17	N	Native	LID#	+3VSUS
GPIO 18	N	Native	USB_OC#0	+3VSUS
GPIO 19	N	Native	USB_OC#1	+3VSUS
GPIO 20	N	Native	USB_OC#2	+3VSUS
GPIO 21	N	Native	USB_OC#3	+3VSUS
GPIO 22	N	Native	ACZ_SDIN0_AUD	+3VSUS
GPIO 23	N	Native	ACZ_SDIN1_MDC	+3VSUS
GPIO 24	N	Native		+3VSUS
GPIO 25	N	Native	SMB_CLK0	+3VSUS
GPIO 26	N	Native	SMB_DATA0	+3VSUS
GPIO 27	N	Native	SMB_CLK1	+3VSUS
GPIO 28	N	Native	SMB_DATA1	+3VSUS
GPIO 29	N	Native	SMB_ALERT#	+3VSUS
GPIO 30	N	Native	PCI_PME#	+3VSUS
GPIO 31	N	Native	SIO_PME#	+3VSUS
GPIO 32	N	GPI	EXTSMI#	+3VSUS
GPIO 33	N	Native	SB_RI#	+3VSUS
GPIO 34	N	Native	SUS_CLK	+3VSUS
GPIO 35	N	Native	MII_INTR	+3VSUS
GPIO 36	N	Native	PHY_RXER	+3VSUS

Pin		Use As	Signal Name	Power
GPIO 37	N	Native		+3VSUS
GPIO 38	N	Native		+3VS
GPIO 39	N	Native		+3VS
GPIO 40	N	Native		+3VS
GPIO 41	N	Native		+3VS
GPIO 42	N	Native	PM_CLKRUN#	+3VS
GPIO 43	N	Native	PCI_PERR#	+3VS
GPIO 44	N	Native	ACZ_SYNC	+3VS
GPIO 45	N	Native	ACZ_SDOUT	+3VS
GPIO 46	i	GPO		+3VS
GPIO 47	i	GPO		+3VS
GPIO 48	N/A	N/A	N/A	N/A
GPIO 49	N	Native		+3VS
GPIO 50	N	Native	SB_PANEL_PWR	+3VS
GPIO 51	N	Native	SB_BKL_ON	+3VS
GPIO 52	N	Native	EDID_CLK	+3VS
GPIO 53	N	Native	EDID_DAT	+3VS
GPIO 54	i	GPO		+3VS
GPIO 55	N	Native	A20GATE	+3VS
GPIO 56	N	Native	RCIN#	+3VS
GPIO 57	N	Native	SATA_LED#	+3VS
GPIO 58	N	Native	THRMTRIP#	+3VS
GPIO 59	N	Native	PM_THRM#	+3VS
GPIO 60	N	GPI	PCB_ID0	+3VS
GPIO 61	N	GPI	PCB_ID1	+3VS
GPIO 62	N	GPI	PCB_ID2	+3VS
GPIO 63	N	Native	IDE_PDIAG	+3VS
GPIO 64	N	Native		+3VS

<Variant Name>

ASUSTeK COMPUTER INC

Title : Schematic data

Engineer: CH_LIN

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 47 of 65

R1.0 (Release on 2006/07/26)

R1.10 (Release on 2006/09/07)

1.)Page 4: Change reference name from L1 to L401.

2.)Page 6: DNI R711 because Int. pull-up resister exists in FAN module.

3.)Page 7: Add R704, Q702 prevent leakage current.

4.)Page 20: Change C2056 and C2057 form 27pF to 22pF for ITTI recommendation.

5.)Page 20: Change reference name from X1901 to X2052.

6.)Page 23: Change reference name C4511 -> C2315, C4513 -> C2313, C4512 -> C2312, C4514 -> C2314.

7.)Page 23: Change R2301 size from 0603 to 0402.

8.)Page 29: Change reference name from R3921 to R2921, C4515 to 2915.

9.)Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.

10.Page 34: DNI D704, R3409, R3411 and mount R3408, R3418 for thermal protection.

11.)Page 36: Change reference name from JP3403 to JP3601

12.)Page 36: Change R3622 size from 0402 to 0603.

13.)Page 20: Change C2062 and C2071 form 15pF to 18pF for ITTI recommendation.

14.)Page 45:Add L4506 and L4507 for EMI requirement.

15.)Page 21: Change BT_LED_EN from GPIO6 to GPIO7, GPIO6 is reserve for VBIOS.

16.)Page 16: Change R1604, R1605 from 0ohm to 33ohm ,C1607, C1608 from 47PF to 10PF ,prevent large overshoot and undershoot.

17.)Page 16: Change L1601, L1602, and L1603 from bead to inductor for tune VGA signal.

18.)Page 19: Add U1951, C1953 to prevent EC second reset from S3.

19.)Page 21: Delete R2174, R2197, R2144, R2152 for no MDC function.

20.)Page 14: Reserve C1423, C1424, C1425 for tune VGA signal and EMI .

21.)Page 13: Mount R1356 for meet NV spec.

22.)Page 23: Change JP2302 footprint .

23.)Page 25: Change C2503 from 0.1uF to 1uF for meet chip spec. Unmount R2504, D2502 for chip can self discharge .

24.)Page 31: Unmount D3104, D3105 ,Add D3120, D3121 for depop (+5VS_AUDIO).

25.)Page 29: Reserve X2953,C2974,C2975,Del R2904,R2921,Add R2903,C2901 for NV AP NOTE .

26.)Page 45: Change L4504, L4505 from 80ohm/100MHz to 120ohm/100MHz for EMI request.

27.)Page 34: Add ESD Protection*D3402 for Touch Pad.

28.)Page 25: Mount D2501 for EMI request.

29.)Page 17: Change +3VS to +3VS_LCD for prevent resume from S3 pannel white noise .

30.)Page 17: Change D1704, R1705 value to meet LCD power discharge sequence.

31.)Page 13&17 : Unmount parts about NEWCARD for no NEWCARD spec.

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer: CH_Lin	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Thursday, September 07, 2006	Sheet 48 of 65	

<Variant Name>

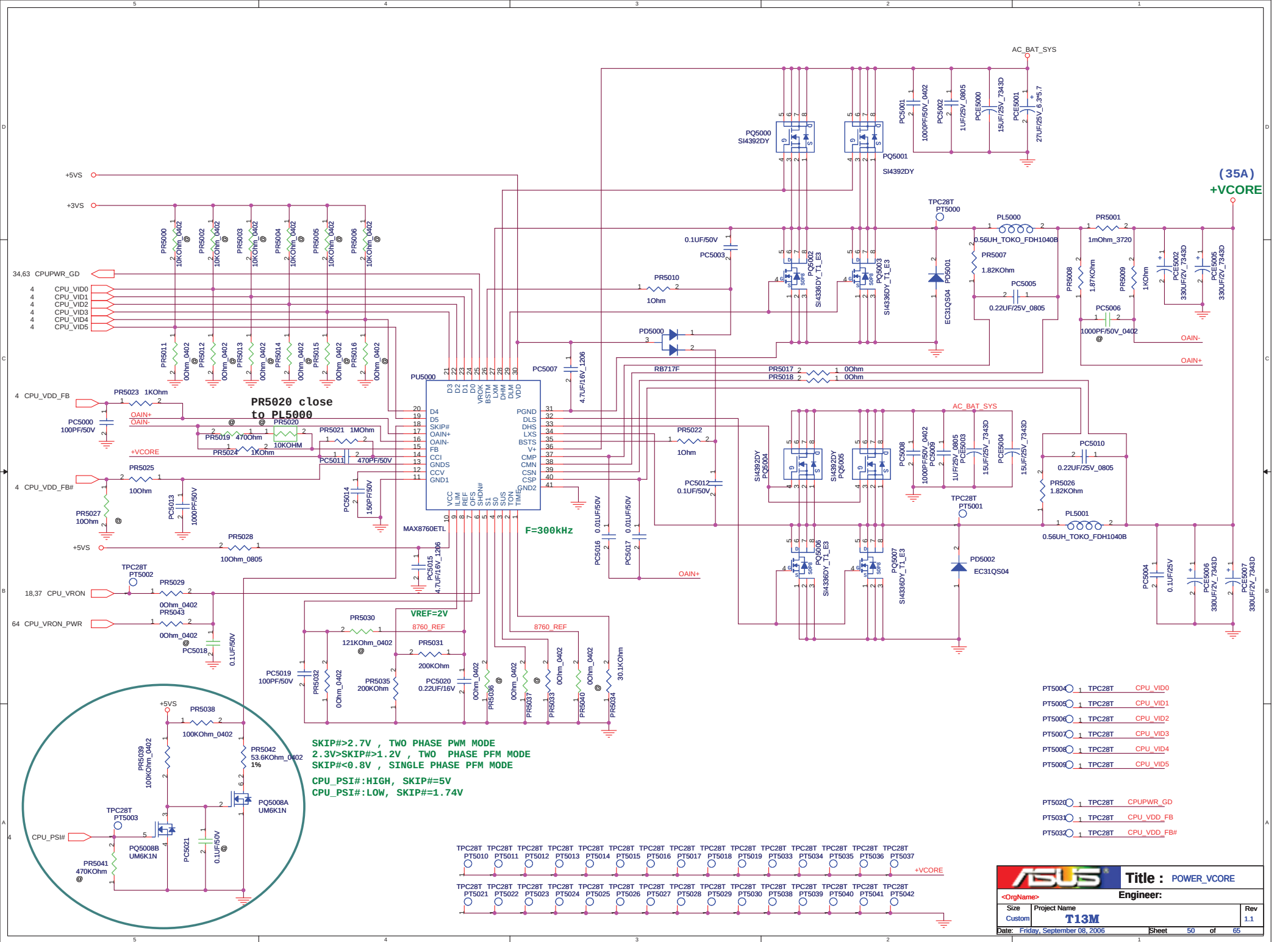
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: CH_Lin

Size	Project Name	Rev
Custom	T13M	1.1

Date: Thursday, September 07, 2006 Sheet 49 of 65



PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)

SR_0728

PU5101B TPS51120RHBR

+5VAO

VCC_TPS51120

PR5101 4.7Ohm

PR5106 12.4KOhm_0402 CS1

PC5111 1000PF/25V

PR5108 9.76KOhm CS2

PC5112 1000PF/25V

PD5101 RB717F

PC5101 10UF/25V_1206

PC5102 1UF/10V

PC5103 1UF/10V

AC_BAT_SYS

+3VAO

PC5100 27UF/25V_6.3*5.7

PC5106 0.1UF/25V

PC5100 0.1UF/25V

PR5102 1Ohm

PC5104 0.1UF/25V

PC5115 10UF/25V_1206

PR5103 1Ohm

PC5107 0.1UF/25V

PC5105 0.1UF/25V

PCE5101 27UF/25V_6.3*5.7

+5VO

+5VSUS (0.1A)

PJP5102 1MM_OPEN_5MIL_G

(5.5A)

PCE5102 100UF/6.3V_7343D

PC5103 100UF/6.3V_7343D

PC5108 1UF/10V

PR5104 22KOhm

PR5105 5.36KOhm

PC5117 1000PF/50V

PQ5101 SI4800BDY

PL5100 4.7UH_#919AS

PD5102 FS1J4TP

PQ5103 SI4800BDY

TPS51120RHBR PU5101A

ENBL

PC5110 1UF/10V

25mil

PR5100 0Ohm

VCC_TPS51120

34,63 SUS_PWRGD

PQ5102 SI4914DY

TPC28T PT5101

PL5101 10UH_#919AS

(5A)

PJP5101 2MM_OPEN_5MIL_G

+3VO

+3VSUS (0.31A)

PCE5105 150UF/4V_7343D

PCE5104 150UF/4V7343D

PC5109 1UF/10V

VCC_TPS51120

PR5107 0Ohm

1000PF/50V PC5116

22KOhm PR5113

PR5114 9.1KOhm

PR5121 100KOhm_0402

PR5119 100KOhm_0402

PR5120 0Ohm_0402

PR5110 0Ohm_0402

PR5111 0Ohm_0402

PR5122 0Ohm_0402

PR5115 0Ohm_0402

PQ5104B UM6K1N

PQ5104A UM6K1N

52,53,61,64 SUSC#_PWR

TPC28T PT5103 PJP5100 1MM_OPEN_5MIL_G +5VA (0.1A)

TPC28T PT5104

TPC28T PT5118 PJP5105 1MM_OPEN_5MIL_G +3VA (0.14A)

TPC28T PT5119

PJP5104 SHORT2

TPC28T PT5105 PT5106 PT5107 PT5108 +5VO

TPC28T PT5109 PT5110 PT5100 +3VO

TPC28T PT5111 PT5112 PT5113 PT5114

TPC28T PT5115 PT5116 PT5117

+12VSUS

AC_BAT_SYS

PC5113 0.1UF/25V

PU5100 MIC5235YM5 IN OUT GND EN NC or ADJ

FB=1.24V

ENBL

PR5116 845KOhm

PC5114 1UF/25V_0805

PR5117 95.3KOhm

TPC28T PT5102

+12VSUS Imax=150mA

VSUS_ON

PD5103 RB717F

PR5118 100KOhm_0402

57 SHUT_DOWN#

7,34,63 FORCE_OFF#

ENBL

+5VAO

PR5124 100KOhm_0402

PQ5105A UM6K1N

34,64 VSUS_ON

PQ5105B UM6K1N

PR5123 100KOhm

ASUS

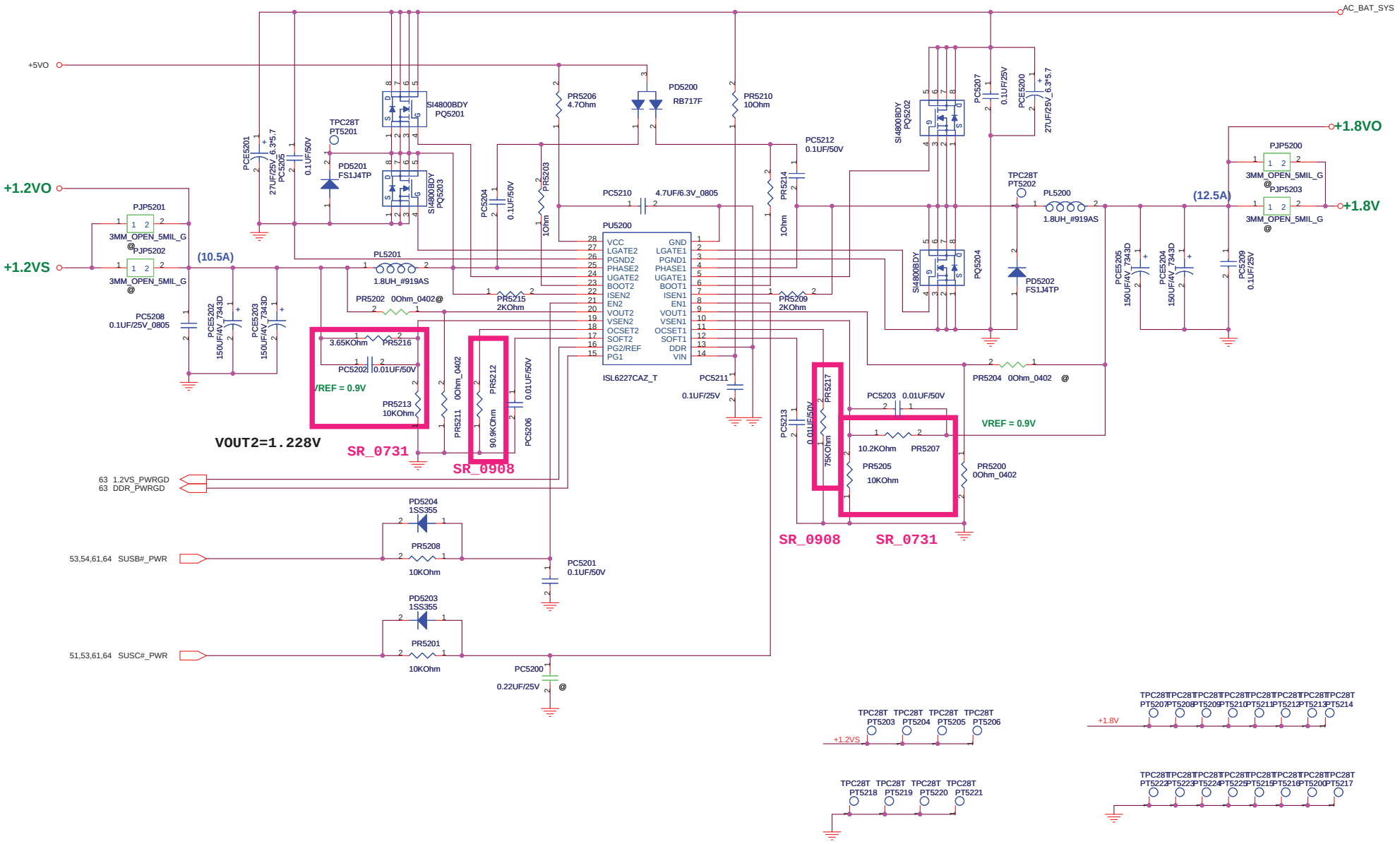
Title : POWER_SYSTEM

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	T13M	1.1

Date: Friday, September 08, 2006 Sheet 51 of 65



ASUS

Title : POWER_I/O_DDR & 1.2VS

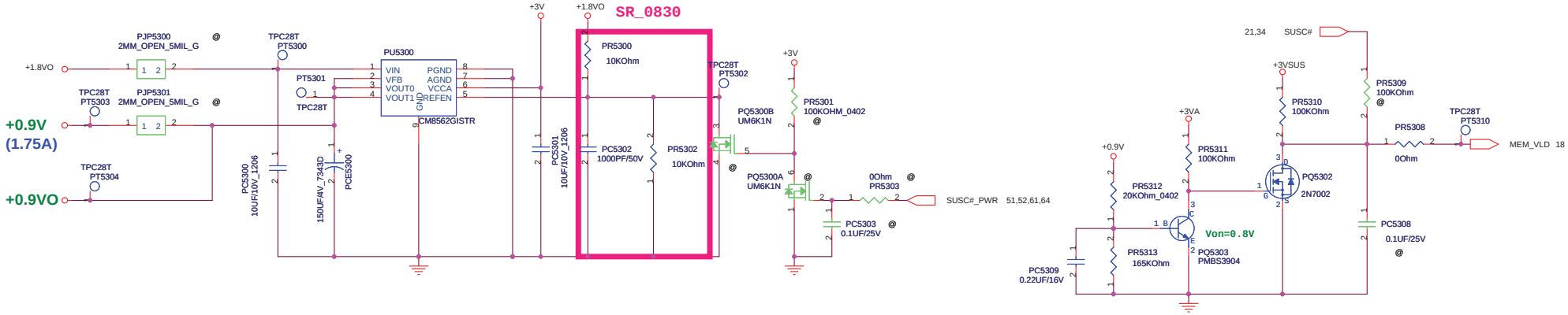
<OrgName>

Engineer:

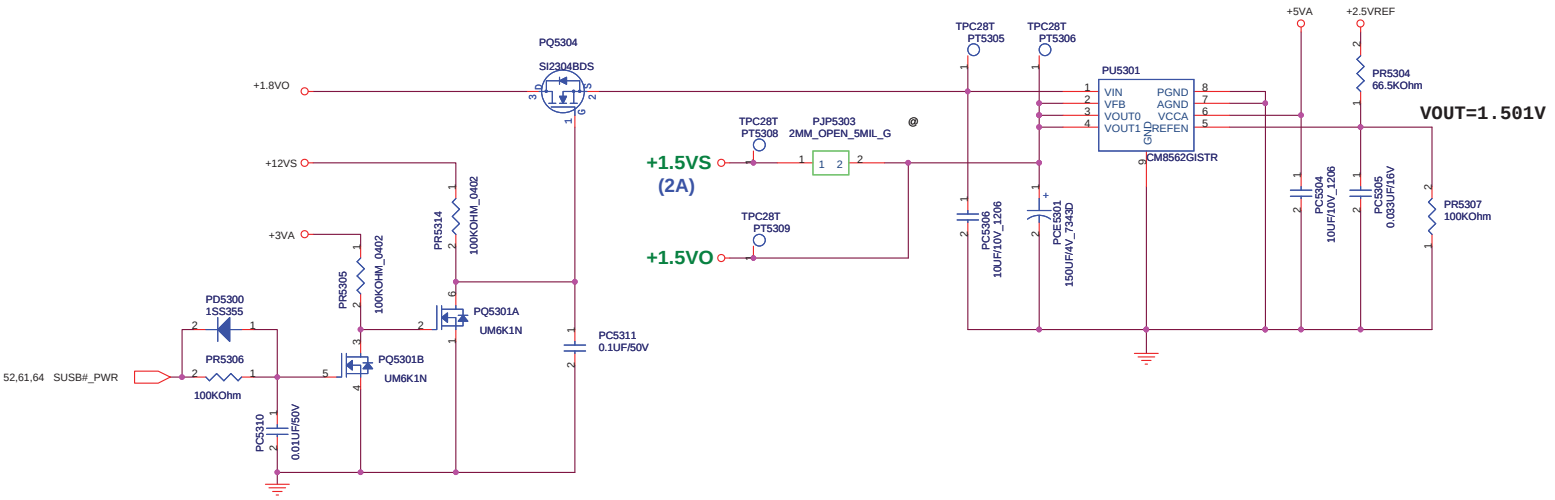
Size	Project Name	Rev
Custom	T13M	1.1

Date: Friday, September 08, 2006 Sheet 52 of 65

VTT

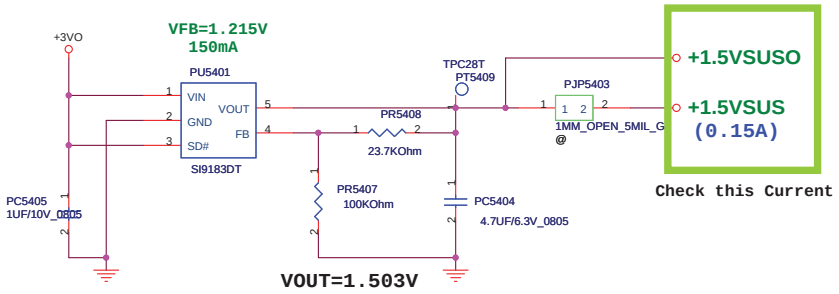


1.5VS

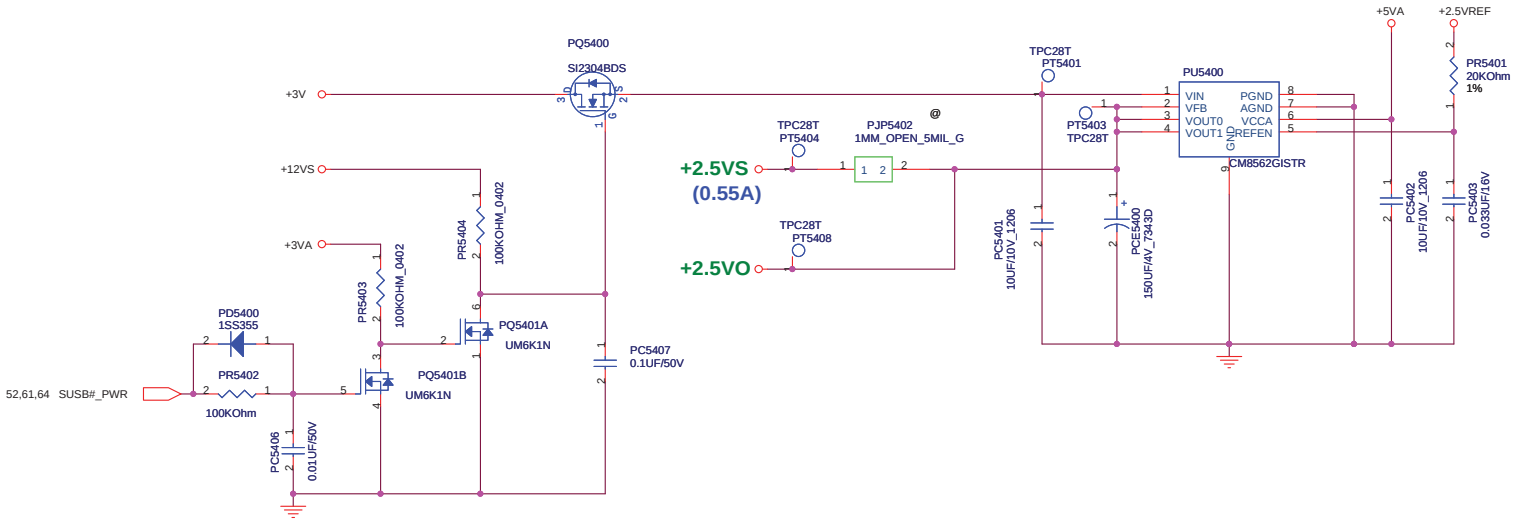


ASUS	Title : POWER_I/O_1.5VS & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 53 of 65	

+1.5VSUS



+2.5VS



ASUS	Title : POWER_+1.5VSUS & +2.5VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 54 of 65	

Title : POWER_VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
C	T13M	1.1

Date: Friday, September 08, 2006 Sheet 55 of 65

Title : POWER_VGA_+1.2VSP

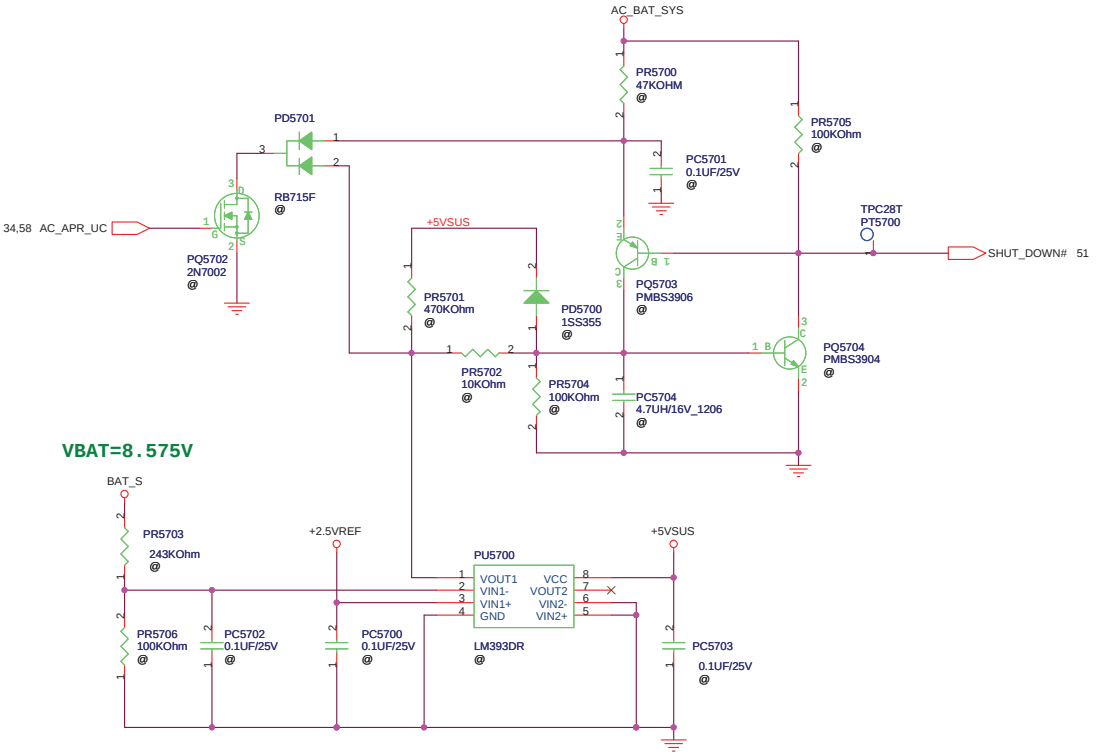
<OrgName>

Engineer:

Size	Project Name	Rev
B	T13M	1.1

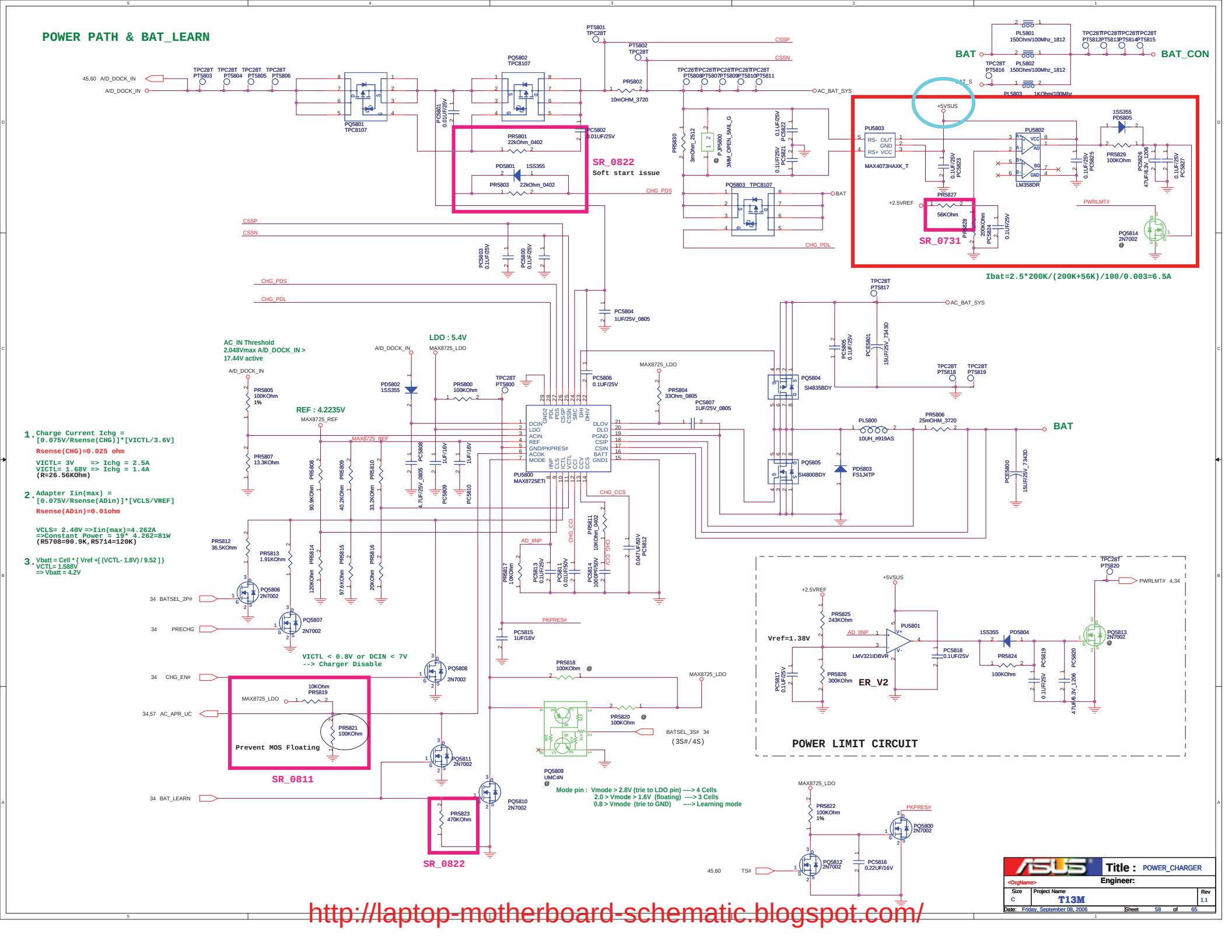
Date: Friday, September 08, 2006 Sheet 56 of 65

BATTERY UVP CIRCUIT



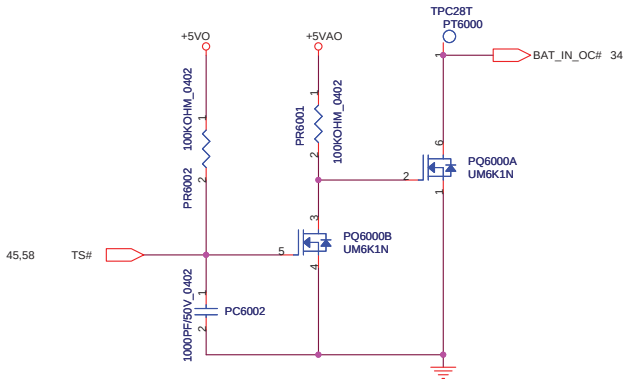
ASUS	Title : POWER_SHUTDOWN#	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 57 of 65	

POWER PATH & BAT_LEARN

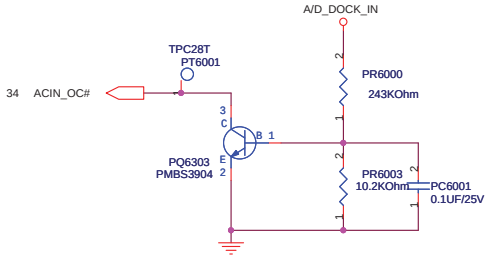


Title :	POWER_PIC
<OrgName>	Engineer:
Size: Custom	Project Name: T13M
Rev: 1.1	
Date: Friday, September 08, 2006	Sheet 59 of 65

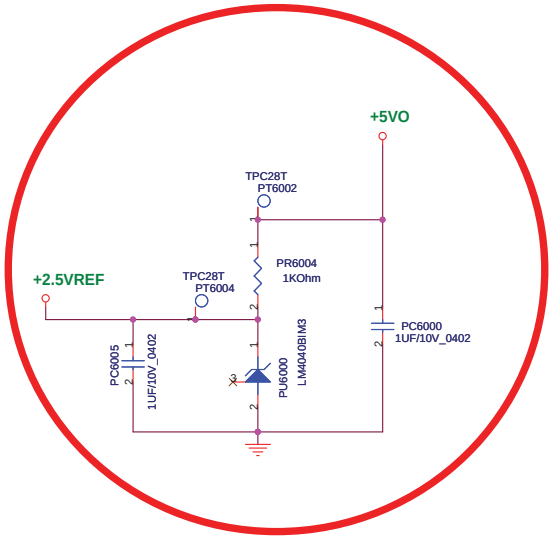
BATTERY IN DETECT



ADAPTER IN DETECT

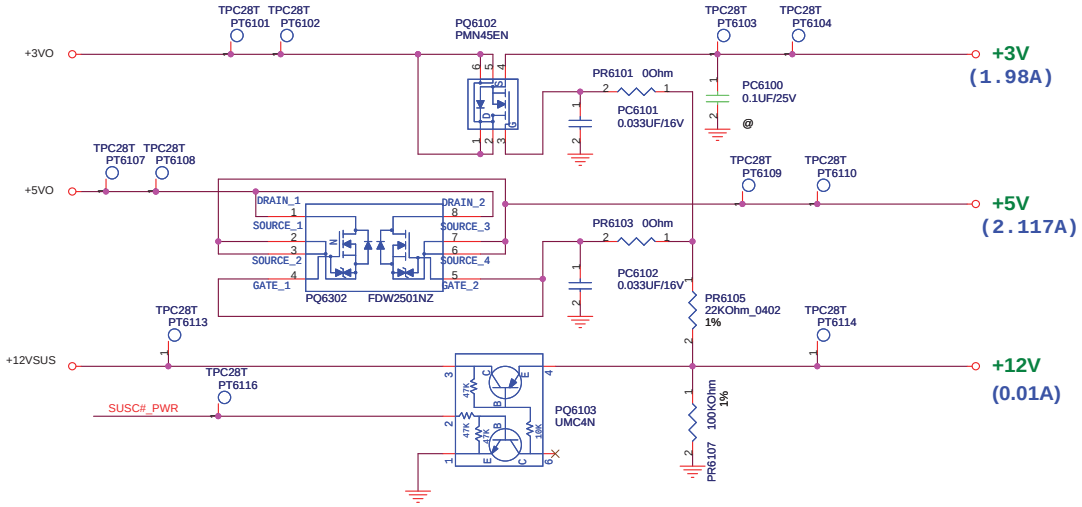


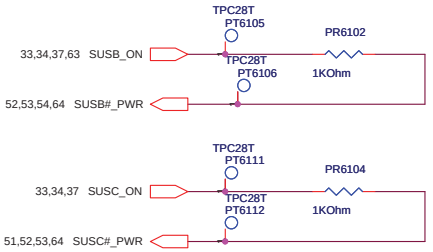
+2.5VREF

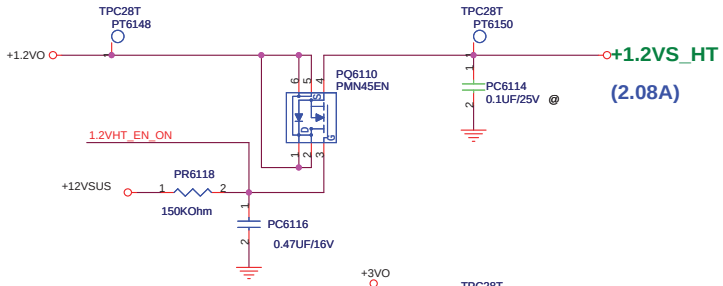


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 60 of 65	

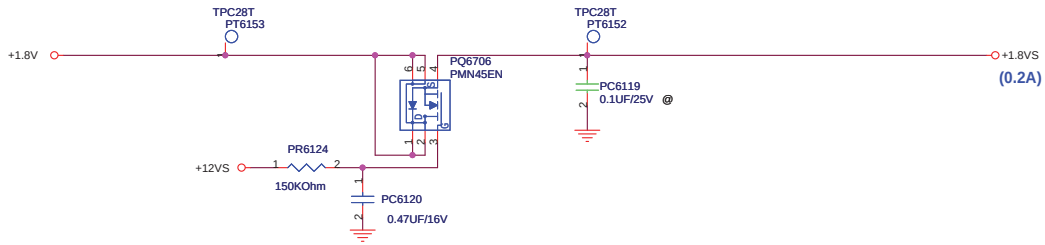
SUSC#_STAGE POWER

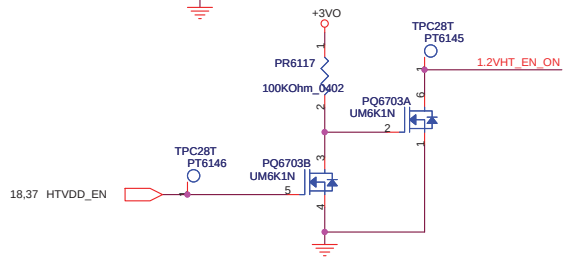


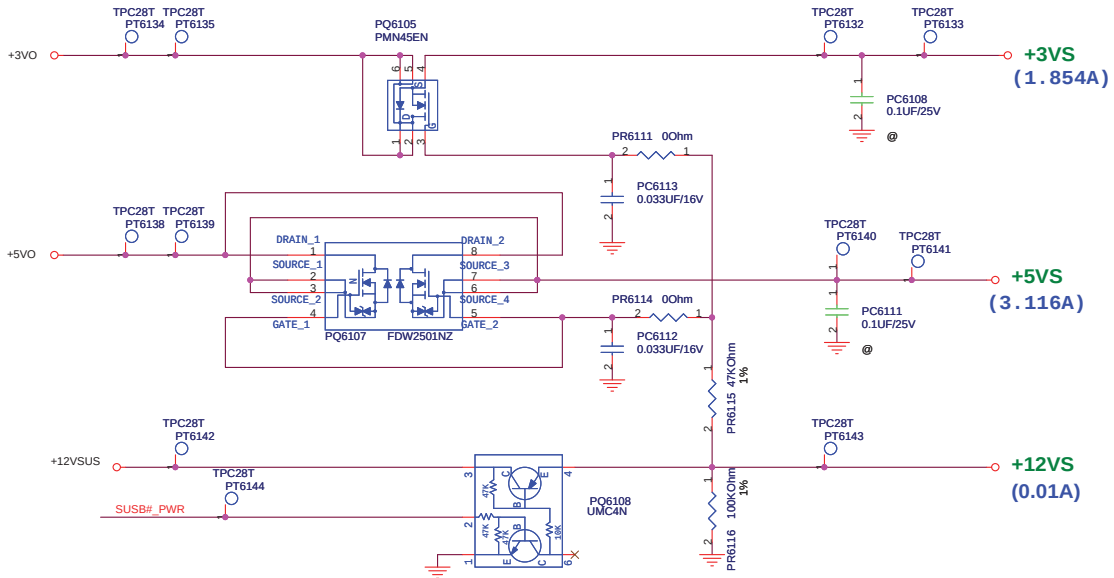


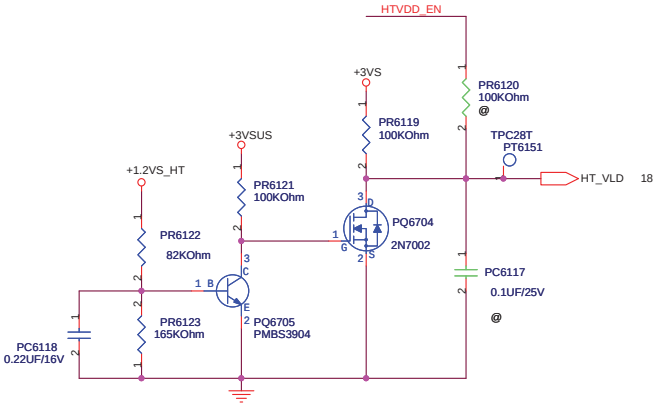


SUSB#_PWR POWER

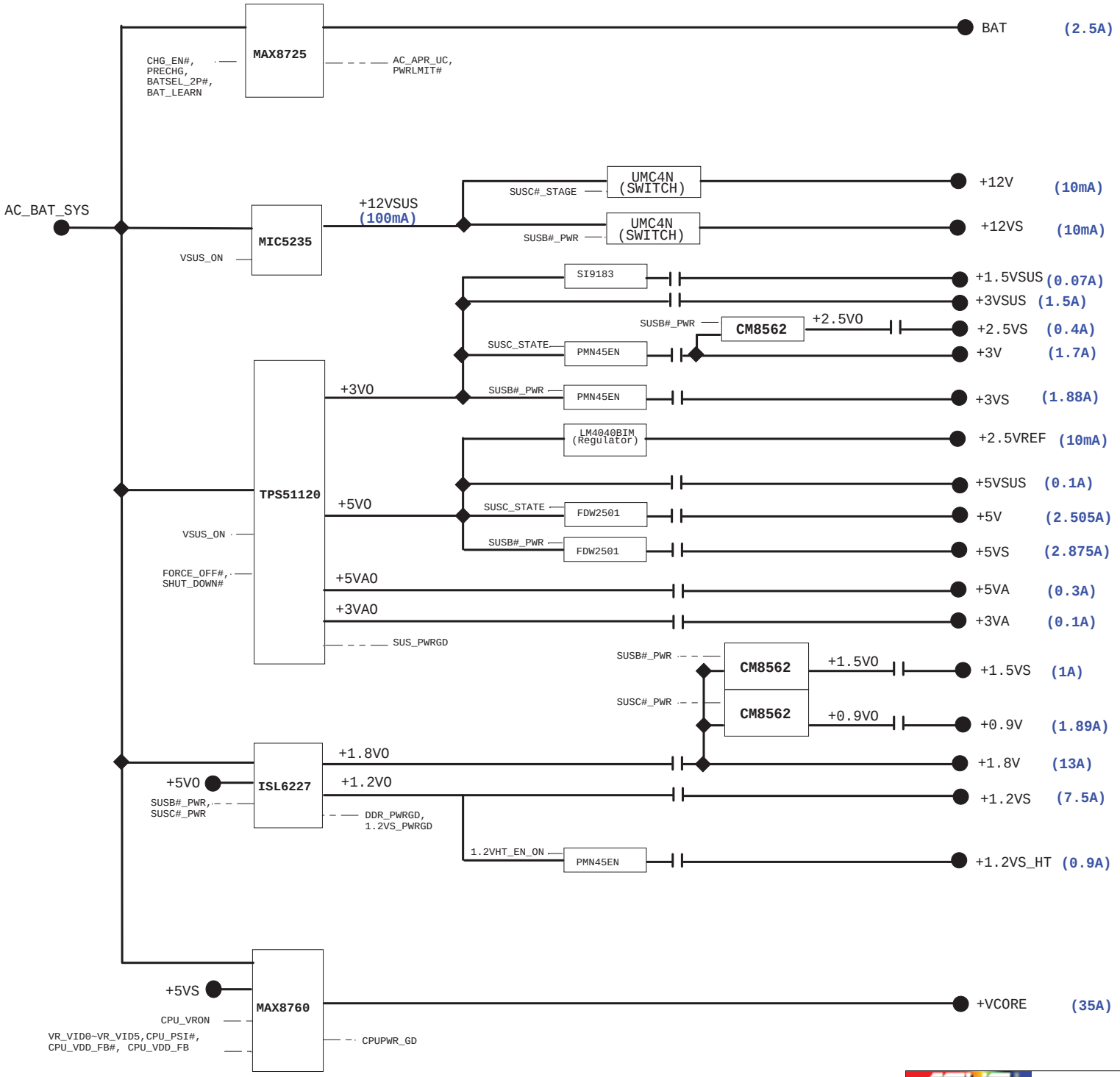








ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 61 of 65	



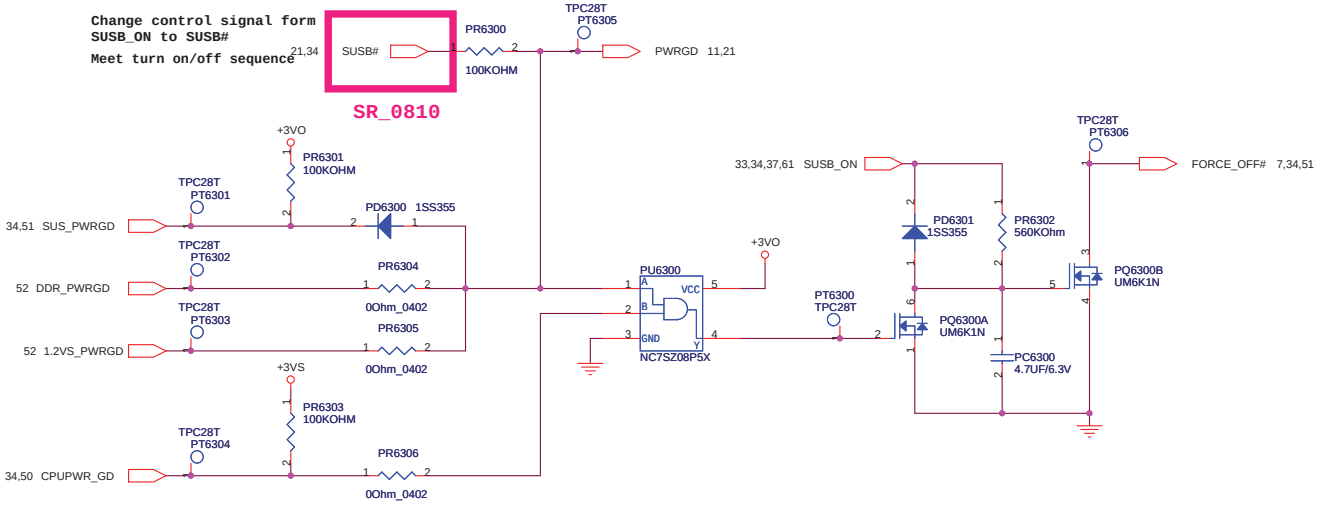
Title : POWER_FLOWCHART

Engineer:

Size: Custom | Project Name: T13M | Rev: 1.1

Date: Friday, September 08, 2006 | Sheet 62 of 65

POWER GOOD DETECTER



PWRGD --> SB --> CPU_VRON

ASUS	Title : POWER_PROTECT	
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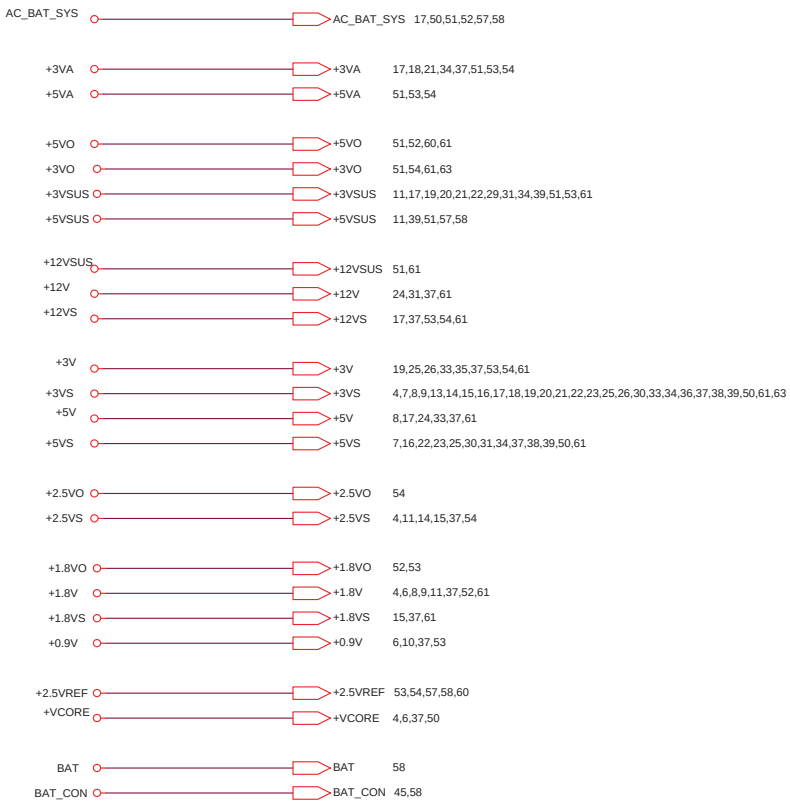
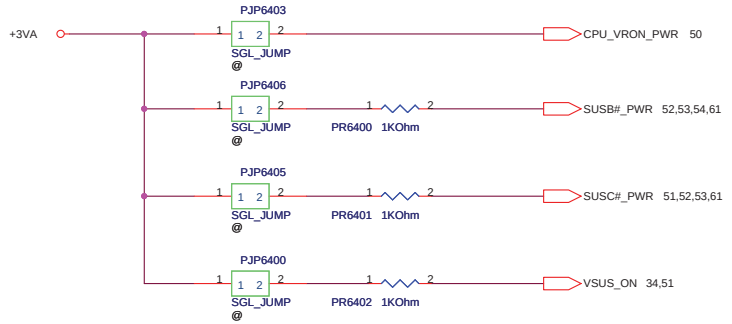
Size: Custom	Project Name: T13M	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 63 of 65	



FOR POWER TEST



ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: ROSA	Rev: 1.1
Date: Friday, September 08, 2006	Sheet 64 of 65	

W2X

Title : History

ASUSTek Computer INC. NB1

Engineer:

Size	Project Name	Rev
Custom	T13M	1.1

Date: Friday, September 08, 2006 Sheet 65 of 65